A DC−48 GHz CMOS All-Digital Frequency Synthesizer for Software-Defined Radios

by

YIN Jun

A Thesis Submitted to
The Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
the Degree of Doctor of Philosophy
in the Department of Electronic and Computer Engineering

January 2013

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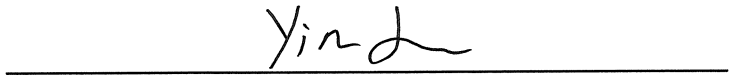

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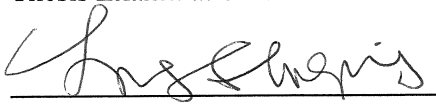

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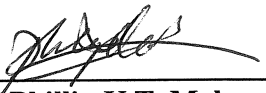

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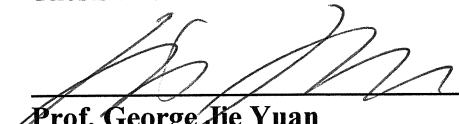

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Abstract

Recently, various communication standards with different carrier frequencies, channel bandwidth, and modulation schemes are widely used every day. The demanding of anywhere and anytime connectivity keeps motivating the industry and academy to find a low cost and low power solution to integrate these different radio access technologies into a portable device with small form factor. Thanks to the continuous scaling down of the CMOS process, which boosts the transistor's unity gain frequency (f_t) to hundreds of GHz, it has been widely used as a low-cost solution for the integration of wireless transceiver systems from radio frequency (RF) frequency to millimeter-wave (mm-Wave) frequency due to its high integration level and high yield. However, the realization of software-defined radios (SDRs) to perform spectrum reception and transmission across multiple decades of frequencies (e.g. from DC to 60GHz) with highly reconfigurable hardware platform in the CMOS process is still of great challenges. In this thesis, a SDR all-digital frequency synthesizer with novel

circuit techniques is proposed in low-cost CMOS process to generate the LO signals from 375 MHz to 48 GHz continuously for the first time.

In the all-digital phase-locked loop (ADPLL) for RF frequency synthesis, firstly, the switched-transformer technique is proposed to implement a triple-band quadrature digitally-controlled oscillator (Q-DCO) in 65-nm CMOS process with an ultra-wide frequency tuning range from 6 to 12 GHz. Secondly, a hybrid phase and time to digital converter (PTDC) is proposed to improve both the time resolution and linearity by using the multi-phase signals divided from the wide-band 6 to 12 GHz Q-DCO.

For millimeter wave (mm-Wave) frequency synthesis, firstly, a multi-mode magnetically-tuned voltage-controlled oscillator (MT-VCO) using a switched-triple-shielded transformer is proposed to increase the frequency tuning range by changing the magnetic coupling coefficient. Fabricated in 65-nm CMOS process, the MT-VCO measures a continuous tuning range of 44.2% from 57.5 to 90.1 GHz and figure-of-merit with tuning range (FOM_T) between -184.2 and -192.2 dBc/Hz. Secondly, the self-frequency-tracking (SFT) technique is proposed to enhance the locking range of injection-locked frequency dividers (ILFDs) without extra power and area penalties. Fabricated in 65-nm CMOS process, the SFT-ILFD prototype achieves an input locking range of 29% from 53.7 to 72.0 GHz and figure-of-merit (FOM) of 9.53.

Finally, the 6 to 12 GHz IQ LO signals generated from the ADPLL is injected into a wideband ×4 injection-locked frequency multiplier (ILFM) with the similar magnetically tuning technique used in the MT-VCO to generate the differential LO signals from 24 to 48 GHz. Followed by two wideband SFT-ILFDs, the12 to 24 GHz IQ LO signals are further obtained. The calibration loop is also proposed to align the free running frequency of the ILFM with 4 times of the injection frequency. From the

measurement results, an SDR frequency synthesizer prototype that can generates IQ LO signals from 305 MHz to 23.25 GHz and differential LO signals from 23.25 to 46.5 GHz with sufficiently good phase noise is successfully demonstrated in 65-nm CMOS process.

Chapter 1

Introduction

1.1 Background

Recently, various communication standards with different carrier frequencies, channel bandwidth, and modulation schemes are widely used by people every day. The wireless communication standards can be cataloged in many ways according to different criterion. According to their communication distances and applications, they can be divided mainly into the following four groups:

- Standards for long-range voice, data, and video transfer: Cellular standards (GSM, EDGE, WCDMA, LTE and etc.) and video broadcasting standards (DVB, DMB and etc.).
- Wireless local area network standards for home and office area connection: 802.11a/b/g WLAN and etc.
- Wireless personal area network standards for short distance connection: Bluetooth, ultra wideband (UWB), 802.15.3c WPAN and etc.
- Other standards not for data transfer or connection purpose such as GPS, RFID and etc.

Another way to catalog the wireless standards is according to their carrier frequency band. In the sequence that frequency goes from low to high. There are video broadcasting standards located from 47MHz to 900 MHz, cellular standards located in around 900MHz, 1.8GHz. Bluetooth and Zigbee located in the 2.4GHz ISM band,

802.11a/b/g WLAN located in both 2.4GHz and 5GHz bands, UWB located in frequency band from 3.1 to 10.6GHz, 802.15.3c WPAN located in frequency band from 57 to 66GHz and the automotive cruise control radar located in 76GHz. It can be seen that the distribution of these frequency bands covers from 47MHz to 80GHz, which is in the range of more than 3 decades.

The wireless communication standards evolve very quickly. To improve the data rates, the new standards either become more efficient in the spectrum utilization by using more sophisticated modulation schemes while still locate in the same frequency band, such as the cellular and WLAN standards as shown in Fig. 1.1 or move to the high frequency to extend the channel bandwidth that can be used, such as the 802.15.3c WPAN located at 60 GHz with 9 GHz bandwidth.

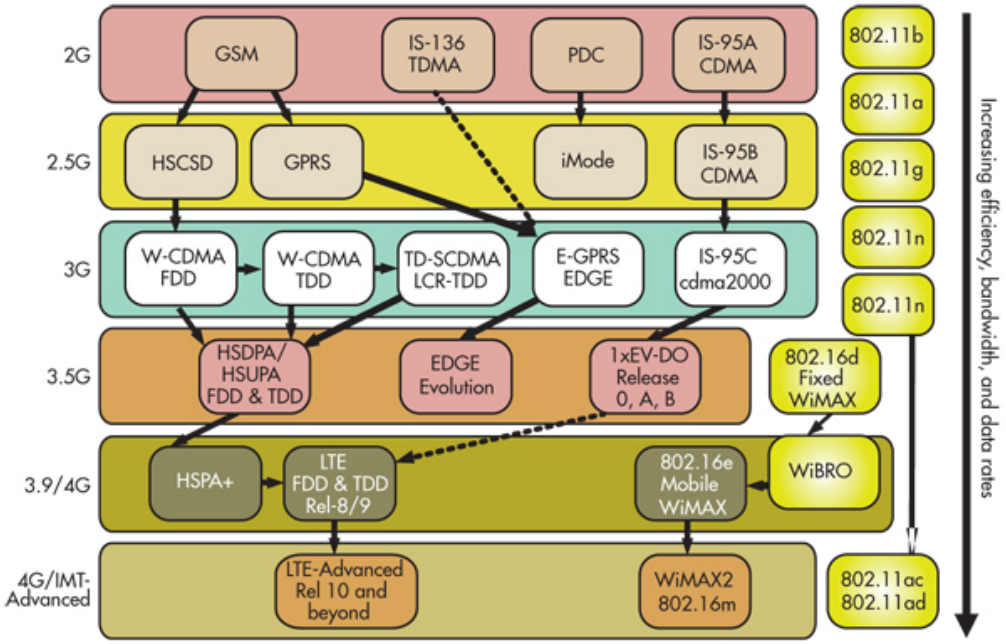

Fig. 1.1 Evolution of the cellular and WLAN standards

1.2 Motivation and Challenges

The demanding of anywhere and anytime connectivity keeps motivating the industry and academy to find a low cost and low power solution to integrate the different radio access technologies mentioned before into a portable device with small form factor. Even though the use of multi-band and multi-standard transceiver ICs [1][2] already helps to reduce the cost and form factor of our cell phones and tablets as shown in Fig. 1.2, they are still a short-term solution in terms of the cost and form factors since they are not fully reconfigurable in the hardware.

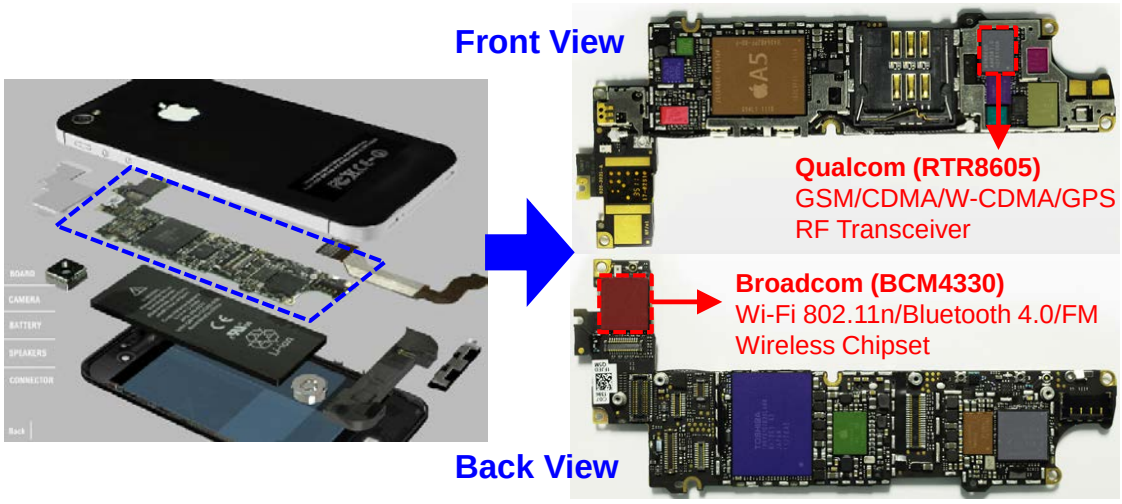

Fig. 1.2 Multi-standard transceiver ICs inside iPhone 4S

Instead of covering only a few existing standards, software-defined radios (SDRs) are proposed to support both all the existing wireless standards and the potential standards in the future, which have the following advantages [3][4]:

- It can support different communication standards with highly reconfigurable hardware platform to minimize the cost and form factor.
- It helps to extend product lifetime due to support new standards with software upgrades. This approach is especially attractive for the rapid growing wireless

industry because both the needs of end-user and standards continue to evolve.

- It can be tailored to specific needs from customer easily for both mass and niche markets.
- It helps to shorten the product's time to market and reduces risks of the new system deployment.

Furthermore, the software-defined radio is also a critical component of the cognitive radio, which can detect and use unoccupied frequency bands to increase spectrum usage efficiency.

Frequency synthesizers as the key block in the SDR transceiver, serve to provide local oscillation (LO) signals with high spectrum purity for the down and up conversion of the incoming RF or mm-Wave signals. To fulfill the requirements from all the standards, the SDR frequency synthesizer needs to be ultra-wide band to generate multi-decade LO signals while still can meet the stringent phase noise and spur requirements from the cellular standards. Besides, the loop bandwidth needs to be reconfigurable to trade off the requirements of in-band phase noise, spur and settling time in different standards. Furthermore, the SDR frequency synthesizer needs to consume low power and occupy small chip area for the applications in the portable device.

1.3 Objective and Contributions of the Thesis

The goal of this research is to study possible ways to build a SDR frequency synthesizer that can cover frequency range from DC to 48 GHz continuously in CMOS process. The frequency synthesizer needs to be reconfigured to meet the requirements of all the wireless communication standards in terms of phase noise, spur and settling time while still maintain comparable performance in terms of power and area when

compared with the frequency synthesizer dedicated to only one special standard. The study will be carried out from the circuit level to system level to see how the innovations in the circuit techniques make such an ultra-wide-band frequency synthesizer system come true. The primary contributions of this thesis are listed below:

(1) The system architecture of an SDR frequency synthesizer that can cover frequency range from DC to 48 GHz continuously is proposed.

(2) The hybrid PTDC architecture is proposed to improve the time resolution and linearity of the TDC while still keeps large input range.

(3) The triple-mode Q-DCO using a switched transformer is proposed to achieve ultra-wide frequency tuning range from 6 to 12 GHz and small frequency resolution at the same time.

(4) The magnetically tuning technique is proposed to greatly increase the frequency tuning range of the mm-Wave frequency VCO. And the systematically design theory is developed.

(5) The self-frequency tracking technique is proposed to enhance the locking range of the ILFDs without the need of extra power consumption and chip area.

(6) The SDR frequency synthesizer prototype is designed, integrated and successfully demonstrated. To our knowledge, it is the very first one that can cover the frequency band from 305 MHz to 46.5 GHz continuously.

1.4 Thesis Overview

The remaining Chapters in this thesis provide further analysis and implementation details of the proposed techniques and are organized as follows.

In Chapter 2, firstly, the requirements on the frequency range, phase noise, settling time and multi-phase LO generation are discussed for different standards. Then the specification of each performance parameter is derived based on the most critical standard. And the existing works for the wide-band frequency synthesizer systems are reviewed. Finally, the system architecture of SDR frequency synthesizer with frequency range from DC to 48 GHz is proposed and the design challenges for individual blocks are highlighted.

Chapter 3 discussed the design of the proposed switched-transformer-based triple-band VCO. The measurement results demonstrate that its frequency tuning range and phase noise can meet the requirements from different standards.

In Chapter 4, firstly, the architecture of the proposed all-digital PLL is introduced. Then the hybrid PTDC is proposed. And the design procedure of the digital loop filter is presented. Finally, the loop dynamics are analyzed by both calculation and behavior simulation.

In Chapter 5, a novel technique to change the coupling coefficient of a transformer tank in a dual-band VCO to significantly increase its frequency tuning range is presented. By exploiting the three states with different magnetic coupling coefficients created by the proposed switched-triple transformer, the stability problem is eliminated and continuous frequency tuning range is achieved. Based on the derived analytical expressions, the design insights and design procedure of this multi-band MT-VCO are also presented. Finally, the experimental results of the 57.5 to 90.1 GHz MT-VCO prototype are presented and discussed.

In Chapter 6, firstly, the locking range limitation of the conventional ILFD is analyzed based on the phasor diagram method. Then a self-frequency-tracking (SFT)

transformer-based injection-locked frequency divider (ILFD) with enhanced frequency locking range is proposed. Finally, the experimental results of the SFT-ILFD prototype with input locking range from 53.7 to 72.0 GHz are presented and discussed.

In Chapter 8, the integration of the whole SDR all-digital frequency synthesizer system is presented and discussed. The millimeter wave frequency generation system is proposed based on a ×4 injection-locked frequency multiplier (ILFM) and two wide-band SFT-ILFDs modified from the MT-VCO and SFT-ILFD in Chapter 5 and Chapter 6, respectively. The frequency calibration loop is employed to align the ILO's free-running frequency with 4 times of the injection frequency to ensure that the injection frequency is always located within the ILFM's locking range. The detailed measurement results are discussed, summarized and compared with the published state-of-art wide-band frequency synthesizer.

Finally, Chapter 9 summarizes this thesis and suggests some future research directions.

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Chapter 2

SDR Frequency Synthesizer Specifications and System Architectures

2.1 SDR Transceiver Architecture

Fig. 2.1 shows the canonical SDR transceiver architect described by J.Mitola [1]. This heavily digitized radio concept can transmit and receive many channels concurrently and provide the highest degree of reconfigurability. However, the front-end ADC and DAC working at the radio frequency requires not only very fast sampling rate (several Gigahertz or even tens of Gigahertz) but also a very large dynamic range because of the complicated block and interference environment, which is still not available now and probably would not be available in the near future. For example, the ADC needs to achieve a dynamic range larger than 99 dB to meet the block requirement specified in the GSM standard as shown in Fig. 2.2. Besides, the estimated power consumption of such high speed, high dynamic range ADC is at the level of hundreds of Watts [2], which makes the Mitola approach not suitable for portable applications.

To reduce the sampling frequency and the dynamic range requirement of the ADC and DAC, we needs to go back to the popular RF front end architectures which down-convert the RF signals to low frequency first by mixing it with the local oscillation (LO) signals. Nowadays, direct-conversion and dual-conversion architectures are two of the most widely used CMOS wireless transceiver architectures [3].

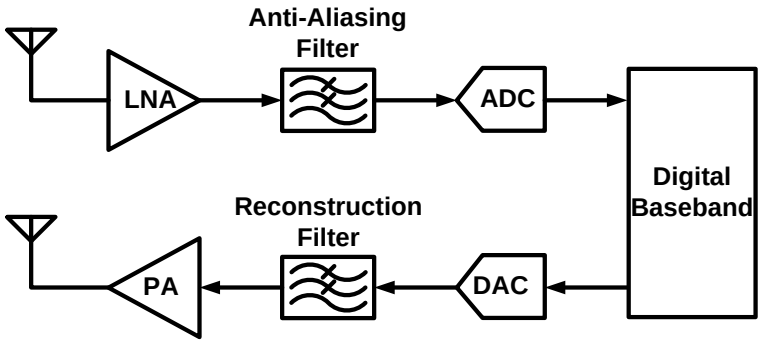


Fig. 2.1 The architecture of the ideal SDR transceiver

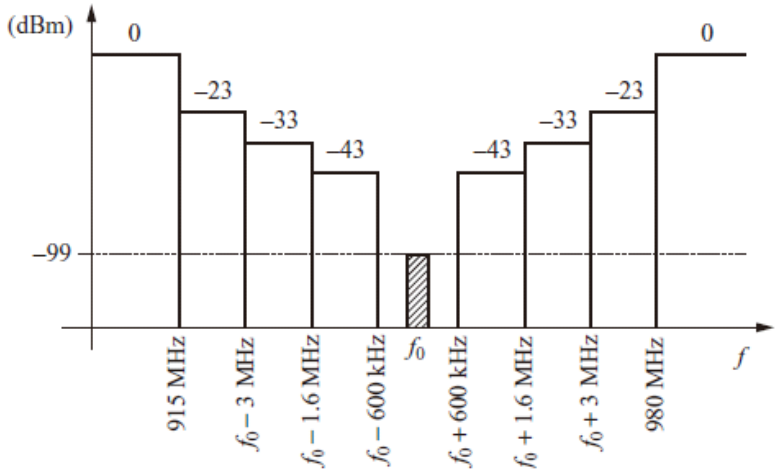


Fig. 2.2 Blocking profile for the GSM standard

Fig. 2.3 shows the direct-conversion SDR transceiver architecture. In the receiver path, either zero intermediate frequency (IF) or low-IF architectures can be employed. For the zero-IF architecture, since the image is the signal itself, no image problem exists and the image reject band-pass filter (BPF) can be eliminated. Besides, the ADC can also operate at low sampling frequency. However, the zero-IF architecture suffers from DC offset which comes from the self-mixing from the LO leakages, strong interferer leaking through the RF port to the LO port, LOs with non-50% duty cycle and even order distortion in the low-noise amplifier (LNA) [4]. LO leakages usually come from two different sources, one is that the LO signal leaks through the LO port to the RF port

due to parasitic couplings and reflect back directly to cause self-mixing. The other one is that the LO signal leaks through the antenna, radiates into the air and then reflects back from the surrounding to be received by the receiver again. Since the DC offset caused by the latter reason is time variant, it is more difficulty to be cancelled compared with these time-invariant DC offsets. Besides, the performance of direct-conversion architecture is also limited by the large flicker noise of MOS transistor in the mixer since it falls in the same frequency band as the output signal after down-conversion. The low-IF architecture is free of the DC-offset problem and can greatly reduce the performance degradation due to flick noise. However, its disadvantages are that the analog to digital converter (ADC) needs to operate at higher frequency and image reject BPF is still necessary before the first mixer. With the scaling down of the CMOS process, the second mixing and channel selection filtering can be moved to digital domain, which adds more flexibility and reconfigurablity to the SDR transceiver.

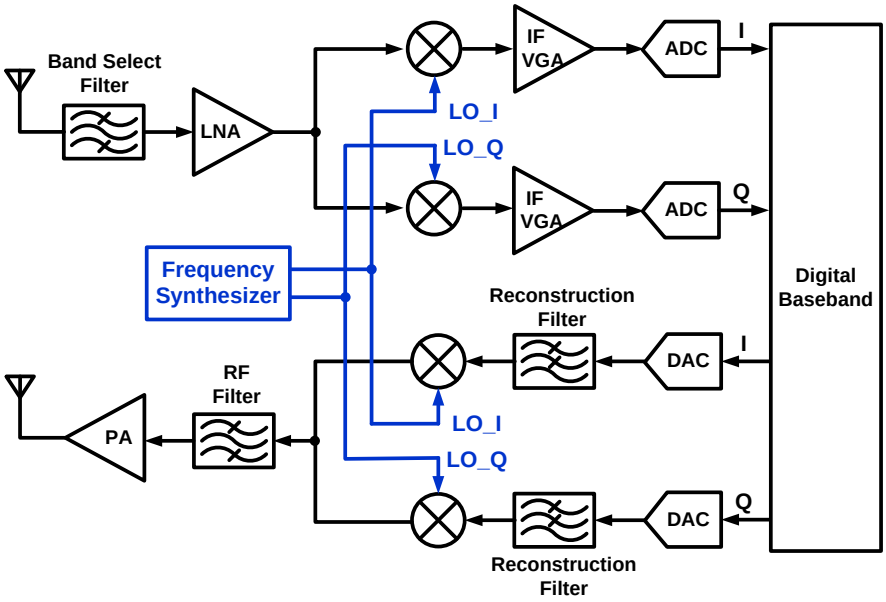


Fig. 2.3 The direct-conversion SDR transceivers Architecture

Fig. 2.4 shows the dual-conversion sliding-IF SDR transceiver architecture [5][6]. In the receiver path, both LO1 and LO2 are used to down convert the input spectrum to an IF and subsequently to DC. Since the LO2 is generated by dividing down the LO1, only a single frequency synthesizer is needed. The typical divider ratio N here is 2 or 4, which indicates that the image frequency is far away from the carrier frequency and is possible to be well suppressed by the on-chip bandpass filtering before RF down-conversion.

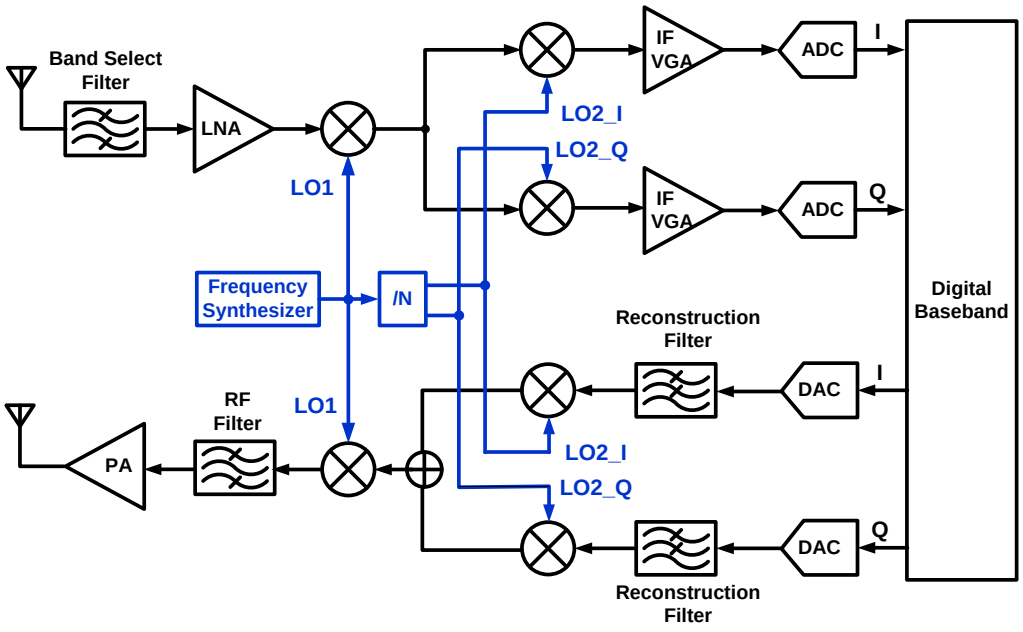


Fig. 2.4 The dual-conversion sliding-IF SDR transceiver Architecture

Compared with direct-conversion zero-IF architecture, firstly, the DC offsets in the dual-conversion sliding-IF architecture is reduced and mostly time-invariant, since the LO emission produced by the receiver is out of the band and also well suppressed by the on-chip bandpass filter. Secondly, since the frequency synthesizer can operate at lower frequency in the dual-conversion sliding-IF architecture, the requirement of voltage-controlled oscillator is relaxed, since it difficult to achieve both large tuning range and

good phase noise performance when oscillation frequency moves up. Thirdly, the matching of the quadrature LO generated at lower frequency is more accurate, which results in lower flick noise of mixers [7].

2.2 General Requirements of Frequency Synthesizers

The frequency synthesizer is the key block in the SDR transceiver systems. It serves to provide the local oscillation (LO) signals with high spectrum purity for the signal down- and up- conversion. Its performance will directly affect the performance of the whole SDR transceiver, and its specifications can also be derived from the requirements of the SDR transceiver. In this section, the general requirements in the design of the frequency synthesizer will be discussed.

2.2.1 Frequency Tuning Range and Resolution

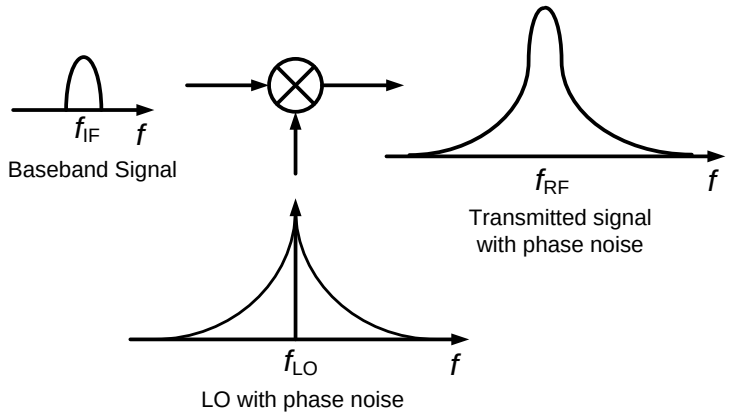
The frequency synthesizer should be capable of frequency tuning since the modern wireless standard usually uses many frequency channels to communicate. For the SDR frequency synthesizer, it needs to cover all the channel frequencies specified by all the standards. For example, if the SDR frequency synthesizer can cover the frequency range from DC to 48 GHz, which means it can fulfill the requirements of the standards located in the frequency from DC to 48 GHz if using the direct-conversion transceiver architecture. By using the dual-conversion sliding-IF transceiver architecture and assuming $f_{LO1}=2\cdot f_{LO2}$, then even the standards from 48 GHz to 72 GHz can be covered. Besides the frequency tuning range, the frequency resolution or the minimum frequency tuning step of a SDR frequency synthesizer needs to satisfy the minimum channel spacing among all the standards.

2.2.2 Phase Noise

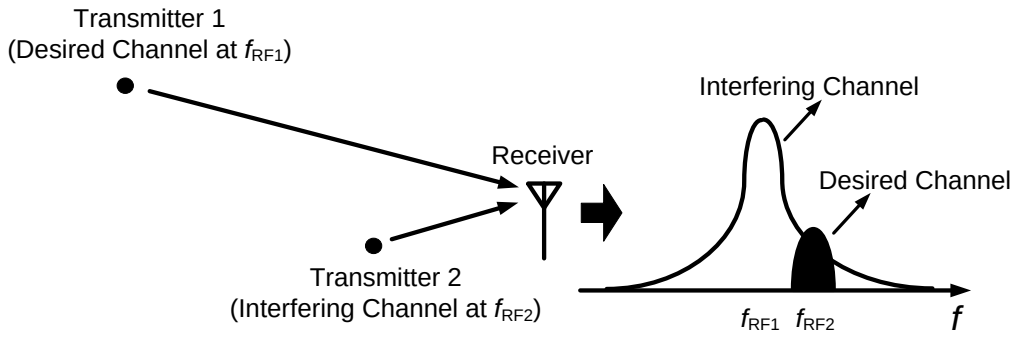
Due to the noise from the transistors in both voltage-controlled oscillator (VCO) and phase-locked loop (PLL), the LO frequency generated from the frequency synthesizer is not a discrete tone in the frequency domain, but rather a tone with phase-noise 'skirts' on both sides as shown in Fig. 2.5 (a). In the time domain, this phase-noise will change the zero-crossing point of the signal which leads to the random jitters. Phase noise is quantified as the ratio between the total noise-power in 1 Hz BW at a specified offset and the carrier power. Both the spot value of the phase noise spectrum at a given frequency offset and the integral of the phase-power spectral density over a given frequency range will affect the transceiver performance.

2.2.2.1 Spot Phase Noise at large offset frequency

During transmission, the transmitted signal from the up-conversion mixing of the IF signal with the LO signal with phase noise will have spectral emissions outside the desired transmit channel. In the scenario that the interfering transmitter is much closer to the receiver than the desired transmitter as shown in Fig. 2.5 (b), the received desired signal would be severely corrupted by the emission from the interfering channel. So the out-of-emission requirement is specified by the wireless standard.



(a)



(b)

Fig. 2.5 (a) Impact of phase noise on the transmitted signal, (b) Near-far transmitters situation

Fig. 2.6. illustrates the transmitter emission requirement. If the mean value of the phase noise over the channel bandwidth can be approximated with the phase noise value at the center point of the channel, the corresponding phase noise requirement at certain offset frequency (Δf_i) can be express as following [8]:

$$\mathcal{L}(\Delta f_i)\left[\text{dBc/Hz}\right] \le P(\Delta f_i)\left[\text{dBm}\right] - P_0\left[\text{dBm}\right] - 10\log\left(\text{Integration BW}\right) \quad (2.1)$$

where $P(\Delta f_i) = P_i$ (i = 1,2,3 ⋯) as shown in Fig. 2.6.

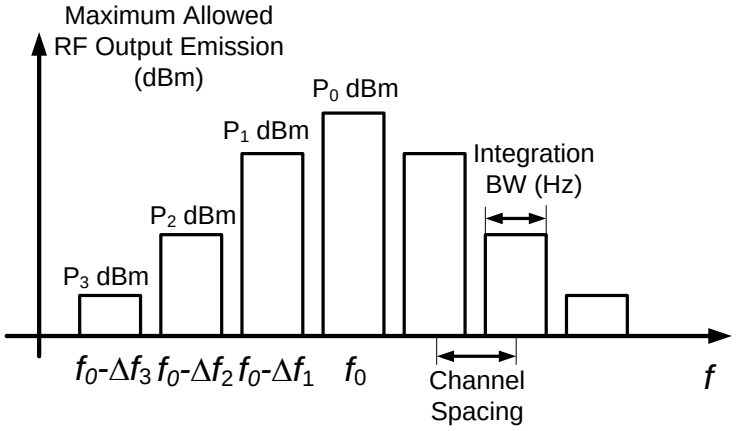


Fig. 2.6 Illustration of the transmitter emission requirement

During reception, as shown in Fig. 2.7, the phase noise of the LO signal will mix with the blockers in the adjacent channels to down-convert them to the same IF

frequency as the desired signal located, which is known as the reciprocal mixing [9]. Given the blocking profile as shown in Fig. 2.8 and using the same flat phase noise assumption over the channel width as that in the transmitter part, the corresponding phase noise requirement at certain offset frequencies (Δf_i) can be express as below [8]:

$$\begin{aligned}&\mathcal{L}(\Delta f_i)\left[\text{dBc/Hz}\right]\\&\quad\le P_{\text{Desired}}\left[\text{dBm}\right]-P_{\text{Blocker}}(\Delta f_i)\left[\text{dBm}\right]-SNR\left[\text{dB}\right]-10\log\left(\text{Channel BW}\right)\end{aligned} \tag{2.2}$$

where $P_{Blocker}(\Delta f_i) = P_i$ ($i = 1,2,3\cdots$) as shown in Fig. 2.8, is the power of the blocker located at frequency $f_0 \pm \Delta f_i$, and SNR is the signal-to-noise ratio which can be obtained from Bit Error Rate (BER) specified in the standard [10].

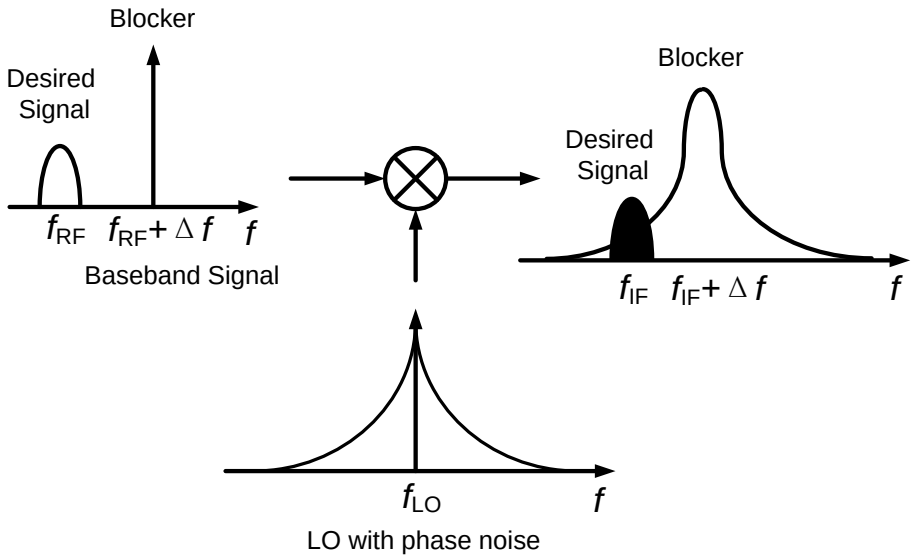


Fig. 2.7 Reciprocal Mixing in the Receiver

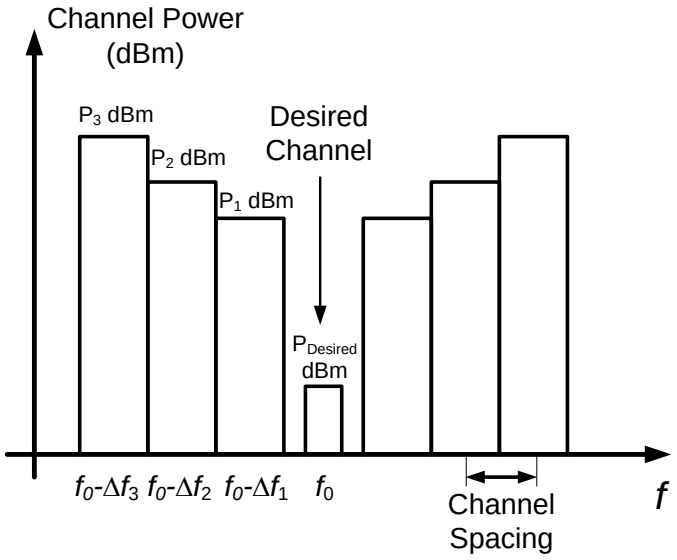


Fig. 2.8 Illustration of the blocking profile

2.2.2.2 Integrated Phase Noise

Even if blockers are not present, the LO phase noise would corrupt the received or transmitted signal and leads to SNR degradation or detection loss [11]. In this case, the SNR will be a function of phase noise power, which is the integral of the LO spectrum. For example, a generic M-QAM modulated signal can be expressed as following:

$$s(t) = \sum_k a_k \cdot p(t - kT) \cdot \cos(\omega_0 t) - \sum_k b_k \cdot p(t - kT) \cdot \sin(\omega_0 t) \tag{2.3}$$

Where (a_k, b_k) are the symbols transmitted in the I/O paths and p(t) is the normalized Nyquist pulse. s(t) can be regarded as an amplitude-modulated and phase-modulated signal with complex envelope $s(t) = (a_k + \mathrm{j}b_k) \cdot p(t - kT)$ at ω_0:

$$s(t) = \mathrm{Re} \sum_k (a_k + \mathrm{j}b_k) \cdot p(t - kT) \cdot \mathrm{e}^{\mathrm{j}\omega_0 t} \tag{2.4}$$

If the LO in the transmitter is affected by phase noise $\phi_n(t)$, then the transmitted signal s(t) will become:

$$s(t) = \sum_k a_k \cdot p(t - kT) \cdot \cos(\omega_0 t + \phi_n(t)) - \sum_k b_k \cdot p(t - kT) \cdot \sin(\omega_0 t + \phi_n(t)) \tag{2.5}$$

or, equivalently:

$$s(t) = \mathrm{Re}\sum_{k}\left(a_k + \mathrm{j}b_k\right)\cdot \mathrm{e}^{\mathrm{j}\phi_{\mathrm{n}}(t)}\cdot p\left(t-kT\right)\cdot \mathrm{e}^{\mathrm{j}\omega_0 t} \tag{2.6}$$

In the receiver part, after down-conversion, coherent demodulation and sampling, the demodulated signal is rotated by $\phi_{\mathrm{n}}(t)$ in the constellation as shown in Fig. 2.9. The same discussion can be applied to the data reception if the LO of the receiver is affected by phase noise.

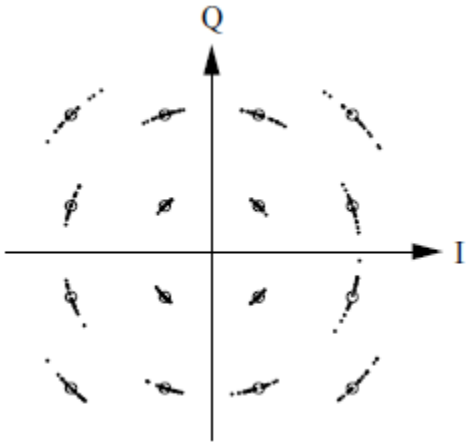


Fig. 2.9 A 16-QAM constellation affected by phase noise [11]

The root mean square (r.m.s.) phase error specified by the standard can be obtained by integrate the LO phase noise:

$$\sigma_{\phi} = \sqrt{\int_{f_1}^{f_2} \mathcal{L}\left(2\pi f\right) df} \tag{2.7}$$

where f is the offset frequency here. The phase-noise power spectral density is typically integrated between frequencies f_1 and f_2. The lower frequency f_1 is set by the bandwidth of a frequency-error correction algorithm, which is typically adopted in the digital base-and subsystem. The upper frequency f_2 is set approximately by the signal bandwidth.

2.2.3 Spurious Tones

Spurious tones are unwanted frequency components in the frequency synthesizer output spectrum which located at certain offset frequency instead of charactering by a distributed spectrum as the phase noise. Since the VCO is essentially a frequency modulator, any periodic signals at the control line of the VCO will result in an output signal with discrete frequency modulation (FM) sidebands.

For the spurious tones at lager offset frequency, the requirement for maximum spur level is similar to that for the phase noise, which can be derived from the transmitter spectrum mask and receiver blocking specification of the wireless communication standards. With the same spectrum power within the channel bandwidth, the influence of spur on the transceiver performance degradation would be roughly the same with that of phase noise. So the spur requirement can be derived by integrating the spectrum density of phase noise within the channel bandwidth [12]:

$$Spur(\Delta f_{\mathrm{i}})\left[\mathrm{dBc}\right] \le \mathcal{L}_{\max}(\Delta f_{\mathrm{i}})\left[\mathrm{dBc/Hz}\right] + 10\log\left(\text{Channel BW}\right) \tag{2.8}$$

where $\mathcal{L}_{\max}(\Delta f_{\mathrm{i}})$ is given by Eq. (2.1) or (2.2).

Besides the influence from reciprocal mixing, the spurious tones present at the offset frequency within channel bandwidth also contribute to the r.m.s. phase error, so it should be included in the integral in Eq. (2.7) when calculating the total integrated phase noise.

2.2.4 Settling Time

The modern wireless communication standards usually have strict requirement on the channel switching time, so the frequency synthesizer needs to settle fast after a frequency step. The settling time is used to define the time required for a synthesizer to

switch from one output frequency to another within a certain frequency accuracy specified by the system requirement [13].

The switching requirements are quite different depending on the wireless standards. In time division multiple access (TDMA) systems such as the GSM, the frequency synthesizer needs to switch between the different frequencies for transmission and reception, and the required switching time is usually in the order of hundreds micro-seconds [14]. In the frequency hopping systems such as WLAN, the channel frequency is changed frequently to make sure that enough packets are received correctly even if some channels within the frequency band would be blocked by very strong interferers. For example, the Bluetooth standard requires a channel switching time of 200 μs and the wireless LAN standard [15][16][17] requires a channel switching time of 224 μs. The faster settling time can be achieved with larger bandwidth, which may degrade the phase noise and spur performance of the frequency synthesizer.

2.3 Specifications of the SDR Frequency Synthesizer System

Table 2.1 shows the specifications of the SDR frequency synthesizer from the wireless standards with the most stringent requirements in terms of the frequency resolution, phase noise and settling time, which are highlighted with bolded text.

Table 2.1 Specifications of the SDR frequency synthesizer

<table>
<tr><th colspan="2">Standards</th><th>Freq. Band</th><th>Channel BW</th><th>Freq. Step</th><th>Phase Noise</th><th>Settling Time</th></tr>
<tr><td rowspan="2">GSM [18][19] [20][21]</td><td>GSM 850/900</td><td>824−960 MHz</td><td rowspan="2">200 KHz</td><td rowspan="2">200 kHz</td><td rowspan="2">-133dBc/Hz @3MHz
-154 dBc/Hz @20MHz

(1.8GHz Carrier)</td><td rowspan="2">870 μs</td></tr>
<tr><td>DCS1800/ PCS1900</td><td>1.71−1.99 GHz</td></tr>
<tr><td rowspan="3">WLAN [15][22]</td><td>802.11a</td><td>5.15−5.85 GHz</td><td>20 MHz</td><td>5 MHz</td><td rowspan="3">-35 dBc (Integrated)</td><td>224 μs</td></tr>
<tr><td>802.11b/g</td><td>2.4−2.484 GHz</td><td>5 MHz</td><td>5 MHz</td><td rowspan="2">224 μs</td></tr>
<tr><td>802.11n</td><td>2.4−2.484 GHz
5.15−5.85 GHz</td><td>40 MHz</td><td>40 MHz</td></tr>
<tr><td colspan="2">Bluetooth (802.15.1) [23]</td><td>2.4−2.479 GHz</td><td>1 MHz</td><td>1 MHz</td><td>-120 dBc/Hz @3MHz</td><td>200 μs</td></tr>
<tr><td colspan="2">RFID Reader [24][25]</td><td>0.86−0.96 GHz</td><td>200−500 kHz</td><td>100 kHz</td><td>-144 dBc/Hz @3.6MHz</td><td>1 ms</td></tr>
<tr><td colspan="2">802.15.3c [26][27]</td><td>57−66 GHz</td><td>2.16 GHz</td><td>2.16 GHz</td><td>-19 dBc (Integrated)</td><td>100 μs</td></tr>
</table>

For the phase noise requirement, the cellular standards (GSM/DCS/PCS) and radio frequency identification (RFID) reader sets the most stringent spot phase noise at the offset frequency outside the channel bandwidth. For comparison, when converted from 900 MHz carrier frequency to 1.8 GHz and from 3.6 MHz offset to 20 MHz offset by assuming 20 dB/Dec slop, the phase noise requirement in RFID reader becomes -153

dBc/Hz, which is 1 dB higher than the -154 dBc/Hz requirement from cellular standard. However, since the phase noise requirement on RFID standard is on the much smaller offset frequency, where the flick noise may degrade the phase noise performance by several dBs easily in the advanced CMOS process, the requirement of -144 dBc/Hz at 3.6 MHz offset frequency from the 900 MHz carrier frequency may be even more difficulty to meet. For the standards with wide channel bandwidth such as 802.11 or 802.15, the reciprocal mixing is no longer a severe problem since the blockers from adjacent channels are located far away from the desired channel and the phase noise at that offset frequency would be quite low. So what we care about is the integrated phase noise. Although the -38 dBc requirement from the 802.11 is much lower than the -21 dBc requirement from 802.15, the phase noise requirement from 802.15 would be even more difficulty to meet considering its carrier frequency is 10 times higher than that of the 802.11 standard.

For the frequency resolution, the RFID reader set the most stringent requirement which requires the LO frequency to be tuned with the finest step of 100 kHz.

For the settling time, as discussed in section 2.2.4, most of the existing wireless communication standards require the channel switch time of several hundreds of micro-seconds. The multi-band OFDM ultra-wide-band (UWB) standard requiring channel hopping time less than 9.47 ns is the only standard not supported by the proposed SDR frequency synthesizer. It is impractical for the frequency synthesizer to settle within such short time since the bandwidth needs to be larger than 1 GHz. If necessary, the proposed frequency synthesizer can be extended to support this standard by using single-sideband mixing method in an open loop manner.

2.4 Review of Existing Wide-Band Frequency Synthesis Systems

The existing wide-band or multi-band frequency synthesizer systems that cover multi-decade frequency range from several GHz to 60 GHz are all based on the architecture which synthesizes the LO in RF frequency based on a RF VCO first and then multiply the LO in RF frequency up to generate the LO in mm-Wave frequency [28] [29]. The reason to use this architecture is that the CMOS mm-Wave VCO can not achieve large frequency tuning range and desired phase noise performance at the same time since the varactor Q drops quickly as frequency goes up. So if the RF LOs are generated by dividing down the outputs from mm-Wave VCOs, then the stringent spot phase noise requirements can not be fulfilled. In the following of this section, the existing solutions of wide-band frequency synthesizer in either RF or mm-Wave frequency will be reviewed and discussed.

2.4.1 Wide-Band RF Frequency Generation

Recently, quite a few researches on the SDR frequency synthesizers working within frequency range from DC to 12 GHz have been reported, since most of the existing wireless standards are located in this frequency range. For the frequency plan, if the VCO can cover the frequency band from $f_{max}/2$ to f_{max}, which is equal to a tuning range of 66.7%, then the frequency from DC to $f_{max}/2$ can be generated by frequency division. In the advanced CMOS process such as 65 nm or beyond, the current-mode-logic (CML) divider works well below 12 GHz, so the bottleneck is at the VCO side, since it is difficulty to design a VCO with 66.7% tuning range from 6 to 12 GHz. When considering the process, supply voltage and temperature (PVT) variations, the tuning range would be even larger than 66.7% in a practical design.

In [30], the frequency tuning range of VCO is relaxed by using the combination of frequency dividers with different division ratios as shown in Fig. 2.10. However, since the /3 or /5 divider is based on the single-sideband mixing scheme as shown in Fig. 2.11, the in-phase and quadrature-phase (IQ) inputs is necessary. To achieve spur-free outputs, only integer divider ratios can be used, which implies that Quadrature VCO (Q-VCO) operating at a much higher frequency of the desired frequency range must be employed. In [30], to produce frequency range from 1 to 10 GHz, a bi-mode Q-VCO operating at 14 and 17.5 GHz are used. Since the Q-VCO is realized by coupling two VCOs in a ring architecture, the trade-off between the phase noise and the IQ accuracy needs to be considered in the design. Furthermore, the Q-VCO is not efficient in power and area since two coupled two VCO needs to operate simultaneously.

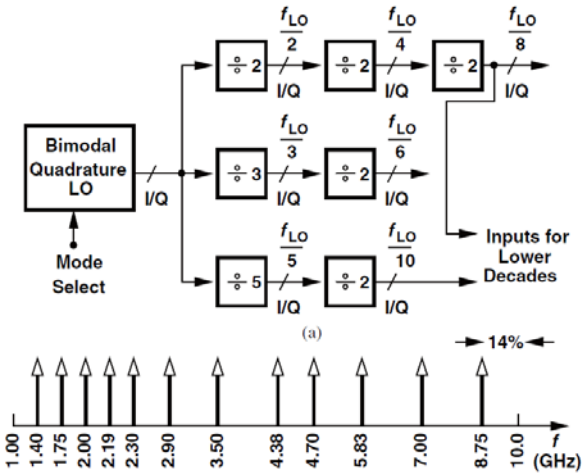


Fig. 2.10 Frequency Plan in [30]

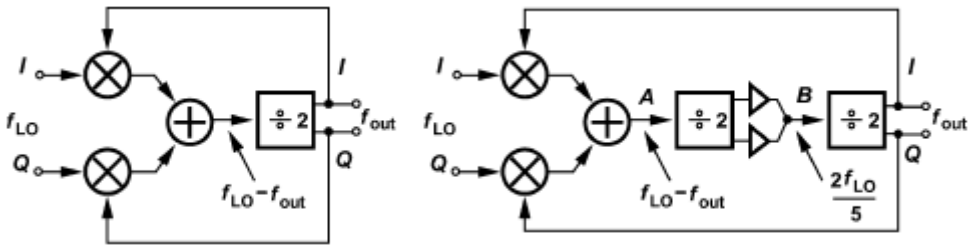


Fig. 2.11 Divide-by-3 (Left) and Divide-by-5 (Right) Schemes [30]

In [28] and [31], the frequency plans are proposed to use only /2 dividers and dual-band VCOs operating at lower frequency. As shown in Fig. 2.12, the low band of the VCO is designed to be located below 6 GHz and the high band is placed higher than 6 GHz. The high band of the VCO output is divided by 2 and then combined with the low band of the VCO output to cover the frequency range from 3 to 6 GHz continuously. Since the low band is directly selected without frequency division, the Q-VCO is still needed to generate the IQ signals.

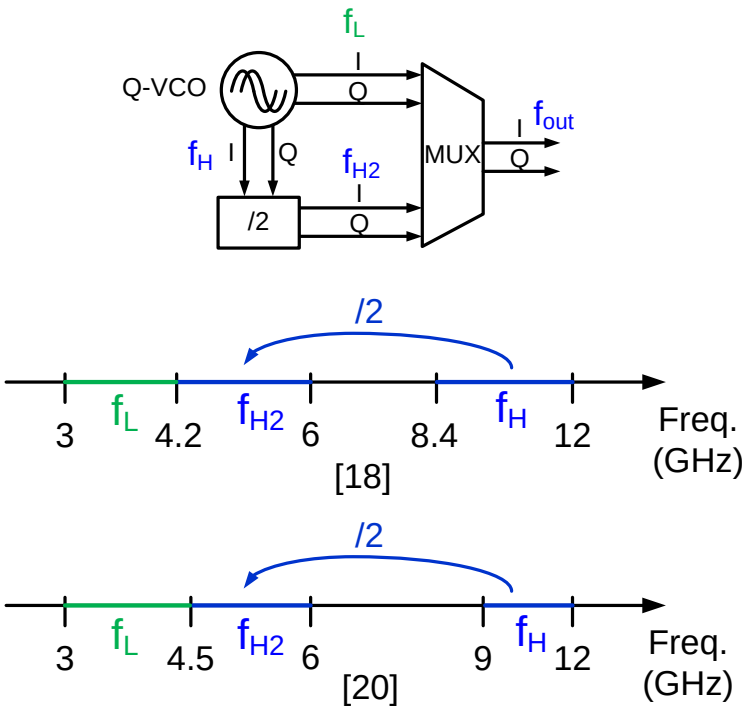


Fig. 2.12 Frequency Plans in [18] and [21]

Compared with the Q-VCO scheme, quadrature LO generation based on the frequency division scheme from differential VCOs (D-VCOs) working at the doubled frequency would dissipate lower power consumption and smaller chip area. However, VCOs working at high frequency suffer from limited tuning range since the parasitic capacitance becomes more dominant. So in [21], two separate VCOs are employed to

generate signals from 5 to 10GHz, which are divided down to obtain quadrature LO signals from DC to 5GHz. However, since the LC VCO with a large inductor is the most area consuming block in the frequency synthesizer, the use of two separate VCO in [21] makes the frequency division scheme less attractive.

2.4.1 Wide-Band Millimeter-Wave Frequency Generation

Currently, the wireless communication standards utilizing the unlicensed 57−66 GHz frequency band for high date rate applications are typically based on the IEEE 802.15.3c specification [26]. As shown in Fig. 2.13, it divides the 9 GHz frequency band into four distinct channels with center frequencies ranging from 58.32 GHz to 64.8 GHz. Its physical layer can support several modulation and coding schemes with different SNR requirements.

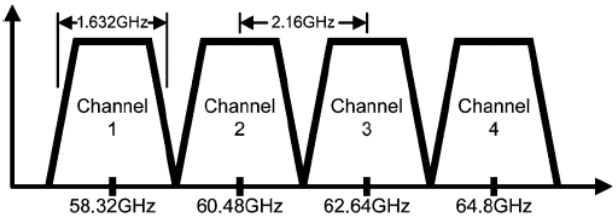


Fig. 2.13 Channel specification of the IEEE 802.15.3c standard

There are several ways to generate the LOs for the IEEE 802.15.3c standard. In both [27] and [32], based on the dual-conversion sliding-IF transceiver architecture, a VCO with fundamental frequency at 2/3 or 4/5 of the channel frequency is employed to generate the first LO, while the second LO requiring quadrature frequency is obtained by dividing the first LO by 4 or 2 respectively. This approach has several design challenges. Firstly, a wide-band VCO is needed to compensate PVT variations. In [27] and [32], the VCO's tuning ranges are from 37.3 to 43.9 GHz and from 42.1 to 53 GHz, which is just cover the required frequency of 38.44 to 43.2 GHz and 46.656 to 51.84

with little margin. Considering a typical +/−10% frequency variation, VCO with increased frequency tuning range is needed. Secondly, the alignment between the VCO's output frequency and the divider's input frequency is difficulty. To avoid complicated calibration scheme, a divider with larger input locking range is needed. Thirdly, since the frequency division ratio between output and the reference (36MHz in [27] and 54MHz in [32]) is very large, the in-band noise contributed by the phase frequency detector (PFD), charge pump (CP) and integrated loop filter needs to be kept very low.

In [28], also based on the dual-conversion sliding-IF transceiver architecture, the 19 to 22 and 38 to 44 GHz IQ LOs are obtained by multiplying up the low frequency around 2 GHz by using the injection-locked multiplier (ILFM) chain. This method eliminates the phase noise contribution from the PFD, CP and loop filter in the PLL loop with large division ratio and will result in a better phase noise performance, since the output phase noise of the ILFM will follow the input phase noise plus $20 \cdot \log N$ within the frequency offset smaller than the ILFM's locking range [34], where N is the multiplication ratio between output and input frequency. However, its disadvantages are also quite obvious. Firstly, the frequency mismatch between each ILFM needs to be properly addressed due to the limited locking range of the ILFMs. Secondly, the output power or the output swing at the two ends of the locking range is low (~0.3V swing at the 40GHz LO output) even with the automatic peak calibration scheme, which requires power-hungry buffers prior to drive the up or down conversion mixers in the transceiver system. Thirdly, each ILFM needs inductor in the tank at mm-Wave frequency, which increases the total chip area.

Due to the narrow band nature of the ILFM with the LC tank, it is difficulty to further extend the frequency range in [28] to continuously cover frequency band from several GHz to 44 GHz. In [29], by using multi-order harmonic injection in low frequency and variable N-push frequency multiplication in high frequency, an output signal from 5 to 32 GHz can be achieve based on a phase-locked input signal of 1 to 1.43 GHz. However, the harmonic injection method suffers from the spurs at the harmonic frequencies [34] of the input and the power of nth harmonic will drop quickly as n increase. As a result, multi-phase signals are needed to boost the desired harmonic while suppress the unwanted ones, which will consume large power. Even with the harmonic suppression scheme, the measured output signal still contains harmonic spurs with relative level of about -50 dB, which is inadequate in many applications. Besides, the output of the N-push frequency multiplication will lose phase information, which means the IQ inputs can only generate differential output through the push-push frequency multiplier. As a result, the 10 to 32 GHz output in [29] has only single phase, which can be hardly used in most wireless transceivers.

2.5 Proposed SDR All-Digital Frequency Synthesizer

2.5.1 System Architecture

Fig. 2.14 shows the architecture of the proposed SDR All-digital Frequency Synthesizer. In the RF frequency generation part, a wideband DCO is employed to generate quadrature LO signals from 6 to 12 GHz and the ADPLL is used to close loop. The /2 divider chain is used to generate LO signals from DC to 6 GHz.

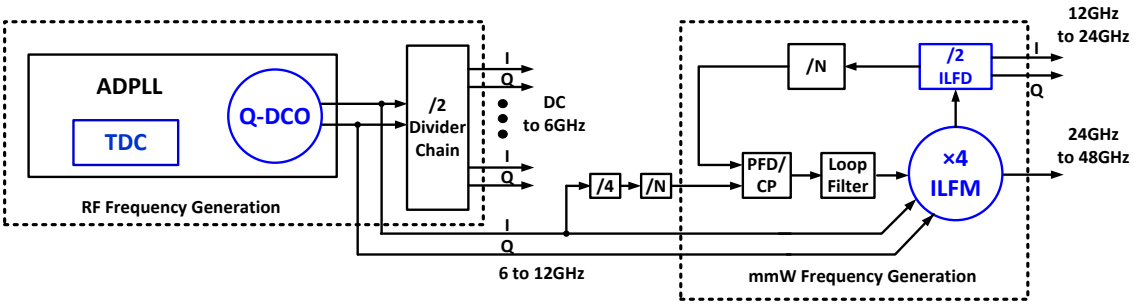


Fig. 2.14 Architecture of the proposed SDR All-digital Frequency Synthesizer

In the mm-Wave frequency generation part, the 6 to 12 GHz IQ signals from the RF frequency generation part is injected into a ×4 ILFM to generate the differential LO signals from 24 to 48 GHz. Since the fundamental and odd number harmonic tones are cancelled by the differential inputs, the output of the ×4 ILFM will only contain the harmonic tones of the desired output signal. Since the input frequency is quite large (6 to 12 GHz), even with mismatch between the input IQ signals and between the differential pairs, the spur closest to the desired output tone will be at least 6 GHz away in the spectrum, which is already out of the frequency band used for the 802.15.3c standard when the generated LOs are used in a dual-conversion sliding-IF architecture. After the ILFM's output, the /2 ILFD will be employed to further generate the IQ LO signals from 12 to 24 GHz. Since the ×4 ILFM itself can not achieve an input locking range from 6 to 12 GHz, so the calibration loop is used to align the free-oscillation frequency of the ILFM to 4 times of the input frequency to guarantee that the input frequency is always within the ILFM 's locking range. The calibration loop can be realized by a phase-locked loop, the output of the /2 ILFD is further divided by 2 to be compared with the reference frequency from the ILFM's input. The calibration and injection can take turns to work at a time division way. At the calibration phase, the inputs to the ILFM are disabled, and the ILFM just runs as a VCO. After the calibration

PLL is locked, the phase frequency detector (PFD) and the charge pump (CP) will be disabled and the large capacitor in the loop filter will preserve the control voltage of the varactor in the ILFM, then the input can be injected into the ILFM.

2.5.2 Design Challenges

The realization of the SDR frequency synthesizer architecture proposed in the last section requires novel techniques on the key building blocks.

(1) The Wideband DCO to achieve wide-frequency tuning range from 6 to 12 GHz and low phase noise (-154 dBc/Hz@20 MHz at 1.8 GHz carrier for cellular standards and -144 dBc/Hz@3.6 MHz at 900 MHz carrier for RFID reader standards) at the same time.

(2) Time-to-Digital Converter (TDC) with fine resolution and high linearity in the ADPLL to reduce the in-band phase noise and fractional spurs.

(3) ILFM with large frequency tuning range is required. To make the frequency calibration scheme work properly, the free-oscillation frequency of the ×4 ILFM needs to be large enough to cover the frequency range from 24 to 48 GHz, which is impossible by using the conventional frequency tuning scheme.

(4) To cover the ILFM's output, the /2 ILFD needs to achieve an input locking range even larger than the ILFM's frequency tuning range.

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Chapter 3

Switched-Transformer-Based Triple-Band VCO

3.1 Introduction

Software-defined radios (SDRs) require LO signals with ultra-wide frequency tuning range over few decades and sufficiently high spectrum purity to support multiple wireless standards. Recently, several schemes to generate wide-band LO signals have been reported [1]-[5]. In [1], two separate VCOs are employed to cover a wide frequency range from 4 to 10GHz, which requires two separate inductors and thus large chip area. In [2], the coupled inductors are switched to achieve 8.1 to 15.4GHz frequency tuning range, but the inductor quality factor is degraded because the switches would introduce extra loss when it turns on and off. In [3] and [4], LO generations are based on dual-band VCOs using either a two-coil transformer or a multi-tapped inductor to minimize chip area. However, due to the stability requirement, the two bands are separate far away from each other, which makes the total frequency tuning range not continuous. As a result, complicated frequency plan is needed for the frequency synthesizers. In [14], a single three-coil transformer with small magnetic coupling coefficient is employed to cover the frequency range from 1.3 to 6GHz. However, the large space between each coil for the stability consideration makes the design still not area efficient. Besides, the three outputs are located far away at three different sides of

the transformer in the layout, which brings difficulties to combine them together at high frequency considering the significant loss of the signal across a long line.

In this thesis, a compact wide-tuning range triple-mode VCO based on a single switched-transformer is proposed. By using common-mode switches, two coils create 3 bands to cover an ultra-wide frequency range from 4.5 to 13.4 GHz, while still maintain low phase noise performance.

3.2 Design of the Switched-Transformer-Based Triple-Band VCO

Fig. 3.1 shows the schematic of the proposed triple-mode VCO and Fig. 3.2 shows the equivalent circuit, and the tank impedance of each mode. The mode selection control table is shown in Table 3.1. LC tanks 1 and 2 together with the common-mode switch (M_{S1}/M_{S2}) between them are employed to create Modes 1, 2 and 3 to cover a frequency band from 4.5 to 13.4 GHz. The outputs of the 3 modes ($V_{o1+/-}$ and $V_{o2+/-}$) are selected by a current-mode-logic (CML) multiplexer.

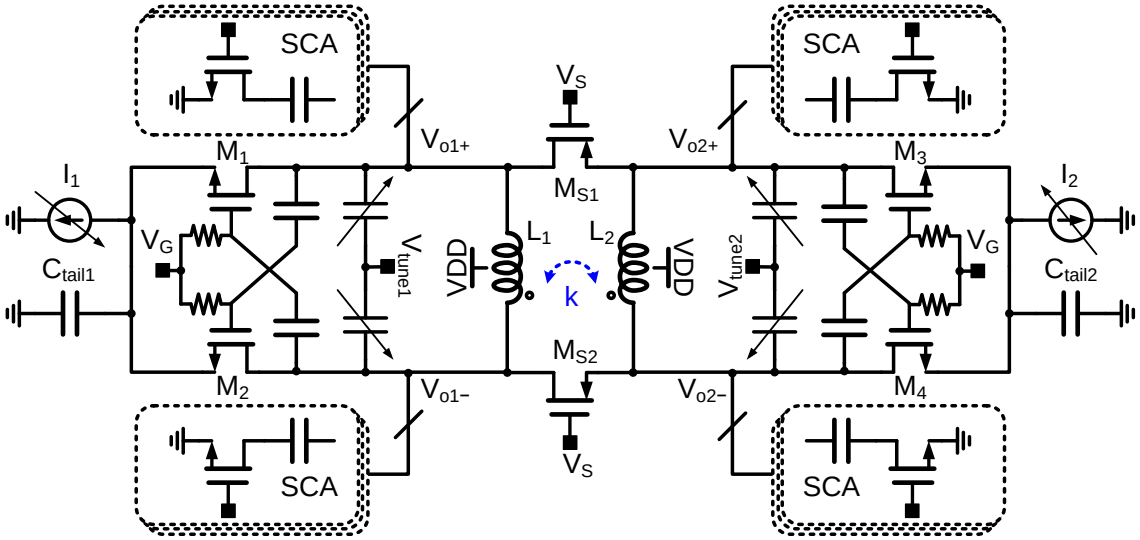

Fig. 3.1 Schematic of the proposed triple-mode VCO

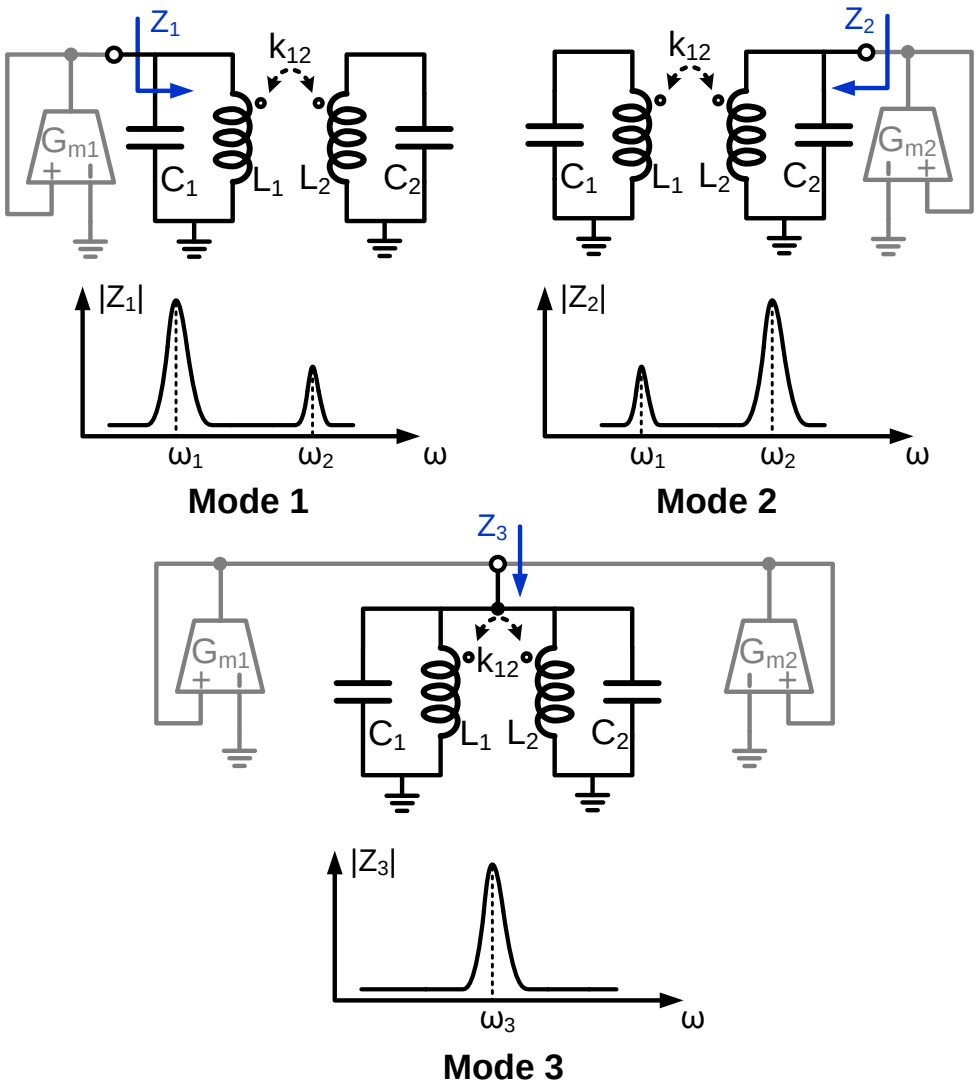

Fig. 3.2 The equivalent circuit and tank impedance for each mode

Table 3.1 Signal control for mode selection

Mode Selection Control			
	I_1	I_2	M_{s1}/M_{s2}
Mode 1	On	Off	Off
Mode 2	Off	On	Off
Mode 3	On	On	On

In Modes 1 and 2, M_{S1} and M_{S2} are turned off, and the oscillator just functions like a normal dual-band VCO. To improve stability condition, the peak frequencies of Mode 1 and 2 are designed far away from each other. The $\omega_2 = 1/\sqrt{L_2C_2}$ is designed to be higher than the $\omega_1 = 1/\sqrt{L_1C_1}$ to ensure the oscillation frequency of Mode 1 much lower than that of Mode 2. When Mode 1 is activated, the switch capacitor arrays (SCAs) of Mode 2 are all off, thus f_2 is set to be 13.4 GHz. When Mode 2 is activated, the SCAs of Mode 1 are all on, thus f_1 is set to be 4.5 GHz. The large frequency separation between f_1 and f_2 also helps reduce the tank impedance degradation due to the dual-mode operation [6]. Mode 3 is created by turning both M_{S1}/M_{S2} on to cover the frequency gap between Modes 1 and 2. In Mode 3, both I_1 and I_2 are turned on. If $L_1 = L_2$ and $C_1 = C_2$, Nodes $V_{o1+/-}$ and $V_{o2+/-}$ become common-mode nodes, which do not degrade the effective tank Q due to the turn-on resistance of M_{S1}/M_{S2}. However, the asymmetry of the two tanks would cause imbalance between the two common-mode nodes, but the effect of the switches' turn-on resistance on the tank Q degradation is still reduced as compared to the case when only I_1 or I_2 is turned on. The sizes of M_{S1}/M_{S2} are chosen to be 120 μm/0.06 μm, which is a trade-off between the turn-on resistance and the parasitic capacitance.

The negative trans-conductance cells for the 3 modes are biased in Class-C with a large C_{tail} to improve the oscillator's phase noise performance for the same power [7]. Fig. 3.3 shows the current injected into the tank in both class-A VCO and class-C VCO with a large C_{tail}. If taking the low band negative-gm cell M_1 and M_2 as an example, then when biased in the class-A without a lagre C_{tail}, the conduction angle for M_1 and M_2 is around π, and the tank current is just a square with 50% duty cycle. So the current magnitude of the first harmonic at ω_0 is $I(\omega_0) \approx (2/\pi)I_B \approx 0.64I_B$, where $I_B = I_1$ or

I_2 in this design. When biased in the class-C with a large C_{tail}, the conduction angle 2ϕ for M_1 and M_2 would be much smaller than π as long as M_1 and M_2 do not enter the deep triode region. Since the current waveforms are now made of tall and narrow pulses, the current magnitude of the first harmonic at ω_0 can be proved to be approximated to I_B [8]. As a result, the class-C VCO with a large C_{tail} only consumes 64% current compared with class-A VCO without a lagre C_{tail} when the same output amplitude is obtained in both cases. Besides, even with the same output amplitude, the class-C VCO exhibits low phase noise performance since the current is injected into the tank at the time period when the largest or smallest output voltage is reached, where the VCO is not sensitive due to the phase disturbance [9]. However, the class-C VCO usually suffers from a slow start-up time, which can be solved by biasing V_B dynamically. During the phase the VCO starts up, the V_B is biased to the supply voltage VDD, which allows a fast start-up time, while the output amplitude exceeds certain voltage level, V_B can be changed to the bias voltage to make the V_{GS} of M_1 and M_2 lower than V_{th}. The auxiliary circuits to dynamically bias the V_B will cause extra power and chip area. However, since the 36% current consumption saving and further phase noise improvement compared with class-A VCO, it is still worthwhile to use the class-C topology.

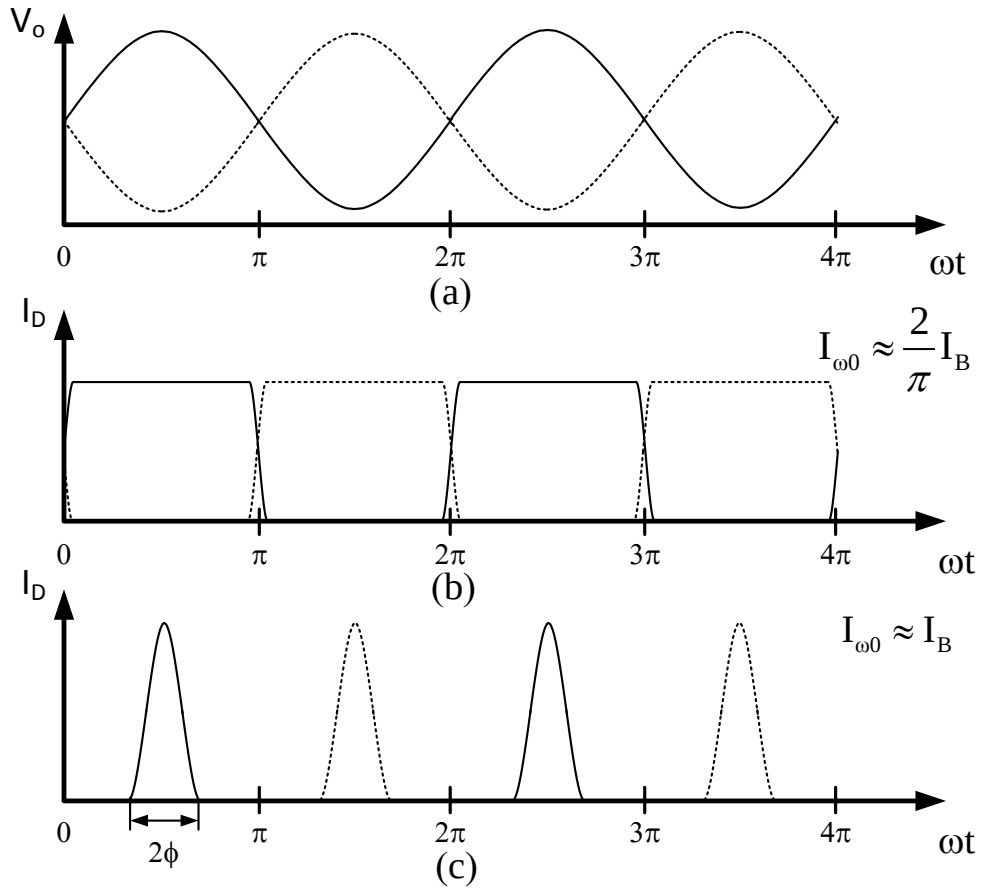

Fig. 3.3 Output voltage and current waveforms in cross-coupled MOS transistors of the VCO: (a) Output voltage, (b) MOS current in class-A VCO (V_B=VDD) and (c) MOS current in class-C VCO (V_B<V_{th}) with a large C_{tail}

The procedure to design the value of L_1, L_2, C_1, C_2 and k is listed as following:

1) Considering there is no coupling between L_1 and L_2, and design L_1, C_1 and L_2 C_2 separately first. Then L_1 and C_1 are chosen based on the minimum and maximum oscillation frequencies desired for the low band in mode 1:

$$\omega_{L,min} = 1/\sqrt{L_1 C_{1,max}} \tag{3.1}$$

$$\omega_{L,max} = 1/\sqrt{L_1 C_{1,min}} \tag{3.2}$$

where $C_{1,max}=C_{1v,on}+C_p$ and $C_{1,min}=C_{1v,off}+C_p$, $C_{1v,on}$ and $C_{1v,off}$ represent capacitance when the switch capacitor array (SCA) and varactor are turned on and off, C_{p1} is the parasitic capacitance from active devices and interconnections. From (3.1) and (3.2), the ratio of $C_{1,max}/C_{1,min}$ can be obtained:

$$\frac{C_{1,max}}{C_{1,min}}=\frac{C_{1v,on}+C_{P1}}{C_{1v,off}+C_{P1}}=\left(\frac{\omega_{L,max}}{\omega_{L,min}}\right)^2 \tag{3.3}$$

The choice of L_1 is the trade-off between phase noise, tuning range and power. The VCO phase noise can be expressed as following [10]:

$$\mathcal{L}(\Delta\omega)=10\log\left[\frac{k_BT}{C}\frac{\omega}{Q_{tank}\Delta\omega^2A^2}(1+\gamma)\right] \tag{3.4}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, C is the tank capacitance, Q_{tank} is the tank quality factor, $\Delta\omega$ is the offset frequency from the oscillation frequency ω, γ is the MOS channel noise factor and A is the output amplitude. It can be seen that larger tank capacitance or smaller tank inductance result in lower phase noise, when the VCO is biased at the boundary of the current and voltage limited range. Besides, the small L_1 also helps to increase the tuning range if C_{p1} and $C_{1v,on}/C_{1v,off}$ are kept constant. However, small L_1 will result in larger power consumption if the output amplitude A is kept the same. By using the same procedure, the value of L_2 and C_2 can be determined. In this design, L_1 and L_2 are chosen to be 800 pH and 580 pH respectively.

2) The choice of k between L_1 and L_2 depends on the stability requirement and the operating frequency of mode 3. When operating in mode 1, the SCA and

varactor in coil 2 are all turned off to make sure $\omega_2 = 1/\sqrt{L_2 C_{2,min}}$ is set to its highest frequency for a large ω_2/ω_1 ratio. Then the k should be small enough to guarantee that even operating at the highest frequency where $\omega_1 = 1/\sqrt{L_1 C_{1,min}}$, the tank peak impedance A_2 at ω_H is small enough that $G_{m1}A_2<1$, where G_{m1} is provided by cross-coupled transistor M_1 and M_2 as shown in Fig. 3.1. When operating in mode 2, the SCA and varactor in coil 1 are all turned on to make sure $\omega_1 = 1/\sqrt{L_1 C_{1,max}}$ is set to its lowest frequency for a large ω_2/ω_1 ratio. Then for the same reason, the k should be small enough to guarantee that even operating at the lowest frequency where $\omega_2 = 1/\sqrt{L_2 C_{2,min}}$, the tank peak impedance A_1 at ω_L is small enough that $G_{m2}A_1<1$, where G_{m2} is provided by cross-coupled transistor M_3 and M_4 as shown in Fig. 3.1.

In mode 3, when switch $M_{S1/2}$ are turned off, the existing of k will result in a larger effective tank inductance than L_1 and L_2 in parallel, which makes it possible to locate the operating frequency in mode 3 between the operating frequency of mode 1and 2. So if k is too small, then the effective tank inductance will drop and the operating frequency will shift up to the operating frequency in mode 2. In this design, k is chosen to be around 0.34.

3) However, when considering the coupling between the L_1 and L_2, the operating frequency ω_L and ω_H in mode 1 and mode 2 will differ from ω_1 and ω_2 as expressed as following:

$$\omega_L^2 = \frac{\omega_1^2 + \omega_2^2 - \sqrt{\left(\omega_1^2 - \omega_2^2\right)^2 + 4k^2\omega_1^2\omega_2^2}}{2\left(1-k^2\right)} \tag{3.5a}$$

$$\omega_H^2 = \frac{\omega_1^2 + \omega_2^2 + \sqrt{\left(\omega_1^2 - \omega_2^2\right)^2 + 4k^2\omega_1^2\omega_2^2}}{2\left(1-k^2\right)} \tag{3.5b}$$

For small k here (~0.34), the difference between ω_1 and ω_L, ω_2 and ω_H are also small. So we can just leave some margin when design ω_1 and ω_2 in the procedure 1), then the real operating frequency ω_L and ω_H will also satisfy the desired frequency tuning range.

3.3 Experimental Results

The triple-mode VCO is fabricated in a 65nm 1P6M LP CMOS process. Fig. 3.4 shows the chip micrograph, which occupies a core chip area of 0.48×0.43mm^2. To obtain the desired value of L_1, L_2 and k specified in last section, L_1 is put as the inner coil with two turns and L_2 is put as a single turn outer coil.

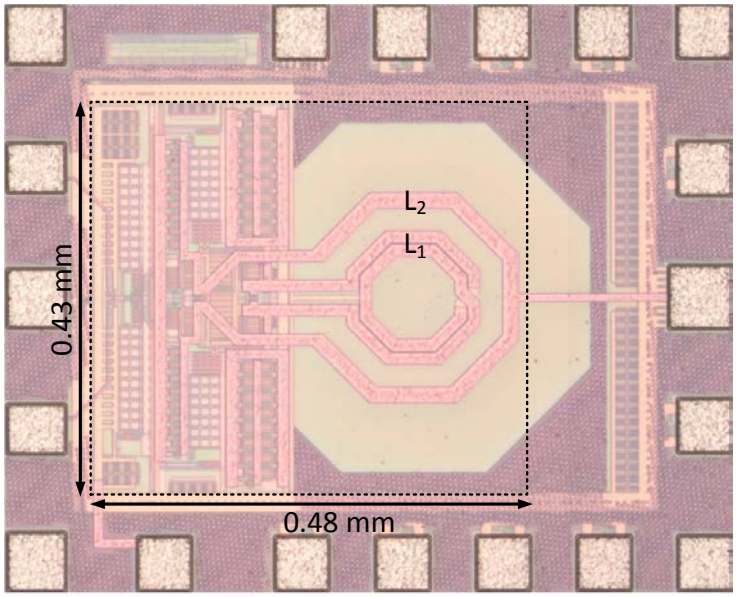

Fig. 3.4 Chip micrograph of the proposed triple-mode VCO

Fig. 3.5 shows the measured frequency tuning range, phase noise, and power consumption of the presented VCO in the 3 modes. Under a 1.2V supply, Modes 1-3 cover a frequency range from 4.5 to 13.4 GHz with enough overlapping and margins. During the measurement, the VCO current is swept to obtain the optimal current value that makes the VCO operating at the boundary between current limited and voltage limited range at each oscillation frequency, which would result in the best figure of merit (FOM).

The measured phase noise of Mode 3 with different I_1/I_2 ratio is plotted in Fig. 3.6. When the summation of I_1 and I_2 is kept constant as 8mA, it can be seen that when both I_1 and I_2 are turned on, the phase noise is improved by more than 1 dB as compared to when only I_1 or I_2 is turned on, which verifies the effectiveness of employing common-mode switches.

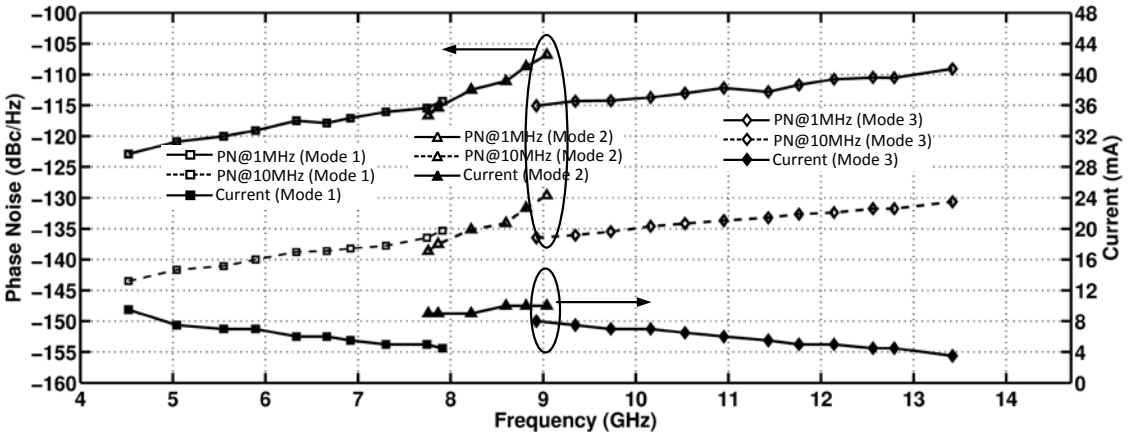

Fig. 3.5 Measured phase noise at both 1 MHz and 10 MHz offsets and current consumption of the VCO in the 3 modes

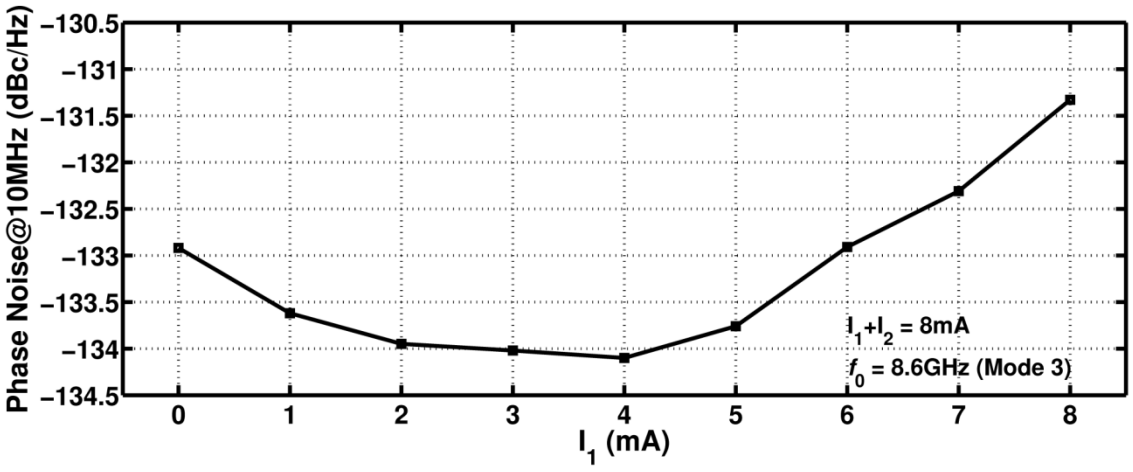

Fig. 3.6 Measured phase noise at 10MHz offset from a 8.6 GHz carrier frequency in Mode 3 as a function of I_1/I_2 ratio

Fig. 3.7 shows the measured phase noise as functions of offset frequency at 7.3 GHz Carrier. The spot phase noise requirements from GSM and RFID standards are also noted. It can be seen that the requirements from both standards are well satisfied.

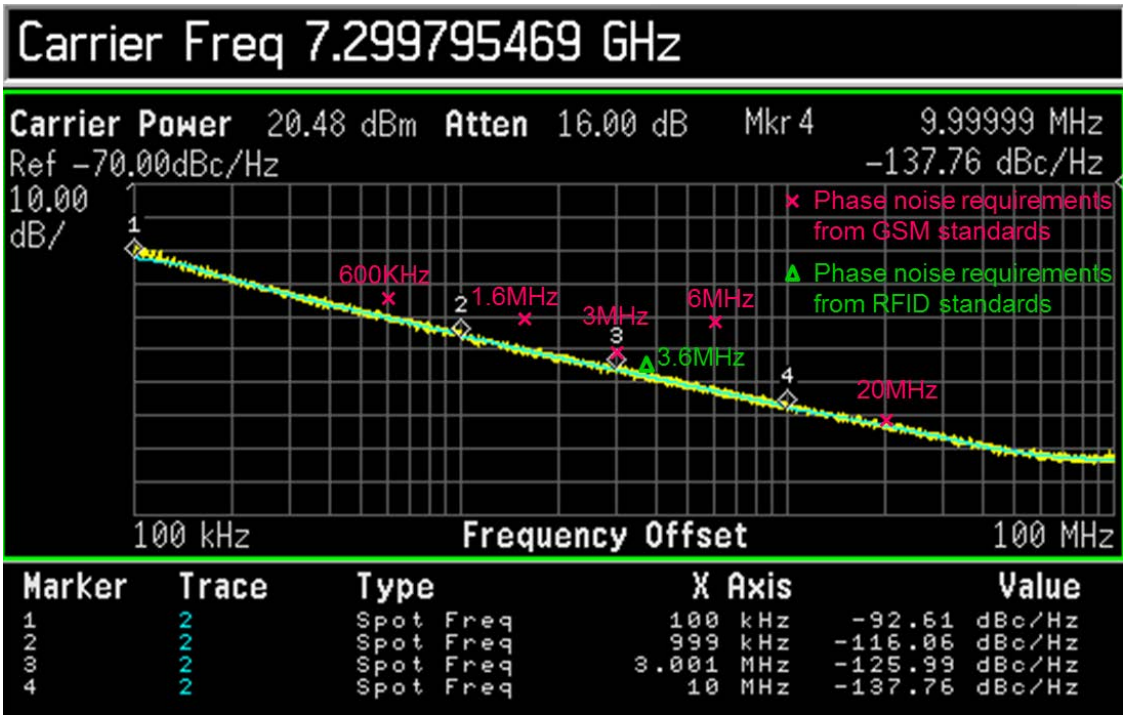

Fig. 3.7 Measured phase noise as functions of offset frequency at 7.3 GHz Carrier

Table 3.2 summarizes and compares the measured performance of the proposed quadruple-mode VCO with that of the recently reported wide-band RF and millimeter wave VCOs. The figure-of-merit (FOM) are defined as:

$$\text{FOM} = \text{PN} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{\text{P}_{\text{diss}}}{1\text{mW}}\right) \tag{3.1}$$

Table 3.2 Performance summary and comparison of the triple-band VCO

	Tech.	Freq. Range (GHz)	VDD (V)	Power (mW)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)	Active Area (mm^2)
[1]	45nm CMOS	4.3 – 10 (80%)	1.1	11	-122@2MHz (f_c=7.2 GHz)	-183	N/A
[2]	90nm CMOS	8.1 – 15.4 (62 %)	N/A	7.67	-106@1MHz (f_c=11.75 GHz)	-179	N/A
[3]	0.13µm CMOS	2.7 – 4.3 (46%)	1.2	18(1)	-136@3MHz (f_c=3.6 GHz)	-185	0.9
		8.4 – 12.4 (38%)		19(1)	-119@3MHz (f_c=10.4 GHz)	-177	
[4]	90 nm CMOS	3.1 – 3.9 (22.8%)	1.2	1.8 to 3.5	-122@2.5MHz (f_c=3.5 GHz)	-182	0.038(2)
		8.8 – 11.2 (24%)		5.6 to 8.3	-117@2.5MHz (f_c=10 GHz)	-179	
[5]	0.13µm CMOS	1.3 – 6 (128%)	1.5	4.35 to 9.15	-117@1MHz (f_c=4.5 GHz)	-181	1(3)
This Work	65nm CMOS	4.5 – 13.4 (100%)	1.2	4.5 to 7.9	-139@10MHz (f_c=6.3 GHz)	-187	0.21
				7.8 to 9.0	-135@10MHz (f_c=8.2 GHz)	-184	
				8.9 to 13.4	-133@10MHz (f_c=11.4 GHz)	-187	

(1) I/Q Outputs, (2) Estimated from layout, (3) With Pads.

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Chapter 4

All-Digital PLL with a Hybrid Phase and Time to Digital Converter

4.1 Introduction

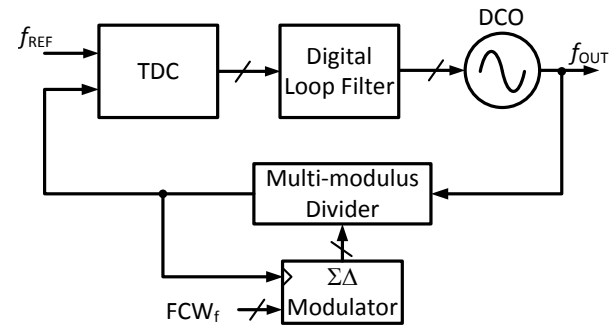
Nowadays, digital-intensive phase-locked loops (PLLs) become more and more attractive in the wireless transceiver system compared with its analog counterparts [1]. Since the time resolution scales favorably with the scaling down of the CMOS process, the in-band phase noise of the ADPLL, which is dominated by the quantization noise is greatly reduced. In an ADPLL, phase is quantized and fed into a digital loop filter. Compared with the analog loop filter which usually requires large capacitor for the low in-band noise, the digital loop filter can leverage the low-power and fast digital processing capability provided by the advanced CMOS process to realize a compact design. Besides, the analog design also suffers from a reduced supply voltage in the advanced CMOS process, while the digital design can take use of it to reduce the power consumption. Furthermore, the digital implementation offers additional advantages such as ease of reconfigurability of loop bandwidth, calibration and ΣΔ noise cancellation. However, the design of an ADPLL is not a trivial work, especially the design of high-performance time to digital converter (TDC).

In this chapter, a digital-intensive reconfigurable 1.5 to 12 GHz ADPLL is presented. By using a hybrid phase and time to digital converter (PTDC) with improved

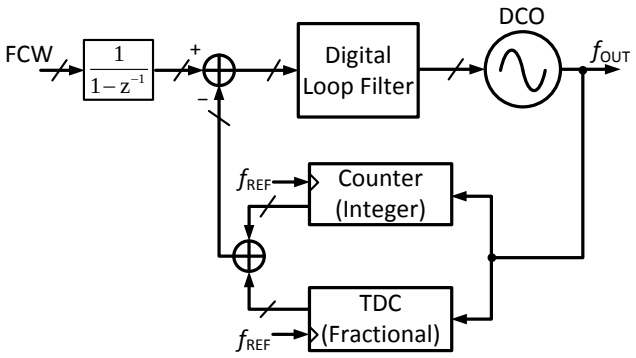
linearity and a wide-band triple-mode digitally-controlled oscillator (DCO), the proposed ADPLL achieves wide frequency tuning range and good noise and spur performance, which makes it suitable to be used in the SDR frequency synthesizer system.

4.2 Architecture of the Proposed All-Digital PLL

There are currently two types of ADPLL architectures which are extensively used for high performance frequency synthesis as shown in Fig. 4.1.



(a)



(b)

Fig. 4.1 (a) ADPLL architecture I with feedback divider, (b) ADPLL architecture II without feedback divider

The architecture I shown in Fig. 4.1(a) is like a conventional analog PLL architecture just with phase frequency detector (PFD), analog loop filter and the VCO being replaced with the corresponding digital versions [2]. Here f_{REF} and f_{OUT} represents the reference signal and the ADPLL output signal, respectively. The frequency control word (FCW) is defined as a combination of integer part (FCW_i) and fractional part (FCW_f), ie., $FCW = FCW_i + FCW_f$. The TDC performs the phase error calculation and the output of which is a digital number proportional to the time difference between reference and divider output edges [3]. The use of the ΣΔ modulators requires a TDC with large input range. For example, if a typical MASH 1-1-1 ΣΔ modulator with 8 levels is used, the input range of TDC needs to be 7 DCO periods (about 2.3 ns for 3 GHz f_{OUT}) to track the time dither induced by the ΣΔ modulator.

The architecture II shown in Fig. 4.1(b) moves the TDC to the feedback path to eliminate the use of frequency dividers [4]. The counter and TDC here measures the accumulated ratio between f_{OUT} and f_{REF}, and by comparing with the integral of the FCW, the digitized phase error can be obtained. Here the input range of the TDC is reduced to only one DCO period. Assuming the same FCW and TDC resolution, the architecture II has the same fractional spur level as that of the architecture I employing a first-order ΣΔ modulator [5].

Fig. 4.2 shows the architecture of the proposed 6 to 12 GHz all-digital PLL. It is based on the architecture II as discussed above. A triple-band DCO modified from the triple-band VCO from Chapter 3, which can cover frequency range from 6 to 12 GHz with margin is employed. The DCO output is divided down by one current-mode logic (CML) divider and one dynamic divider to generate 8-phase inputs (CKV0~CKV7)

from 1.5 to 3 GHz to the frequency counter and the proposed hybrid phase and time to digital converter (PTDC).

As shown in Fig. 4.3, the counter output (Φ_{CNT}) represents the phase of CKV0 normalized to the REF period at the time when the next rising edge of the CKV0 after the rising edge of REF appears. Since what we really want is Φ_{CKV} which is the phase of CKV0 normalized to the REF period at the time when the rising edge of the REF appears, the PTDC is used to measure the phase (or time difference) difference (Φ_{PTDC}) between the rising edge of the REF and the following rising edge of the CKV0. Then $\Phi_{CKV} = \Phi_{CNT} - \Phi_{PTDC}$. If the ADPLL is locked, then Φ_{CKV} needs to be equal to the integral of the FCW ($\sum$FCW), so the phase error (Φ_e) is just the difference between Φ_{CKV} and $\sum$FCW.

The phase error is then sent to the digital loop filter (DLF) to generate the DCO control word. The integer control word INT[9:0] directly controls varactor banks in the DCO while the fractional control word FRAC[13:0] is sent to the ΣΔ modulator first to generate the overflow control OF[2:0] to dither the varcators in the DCO, which results in a fine frequency resolution.

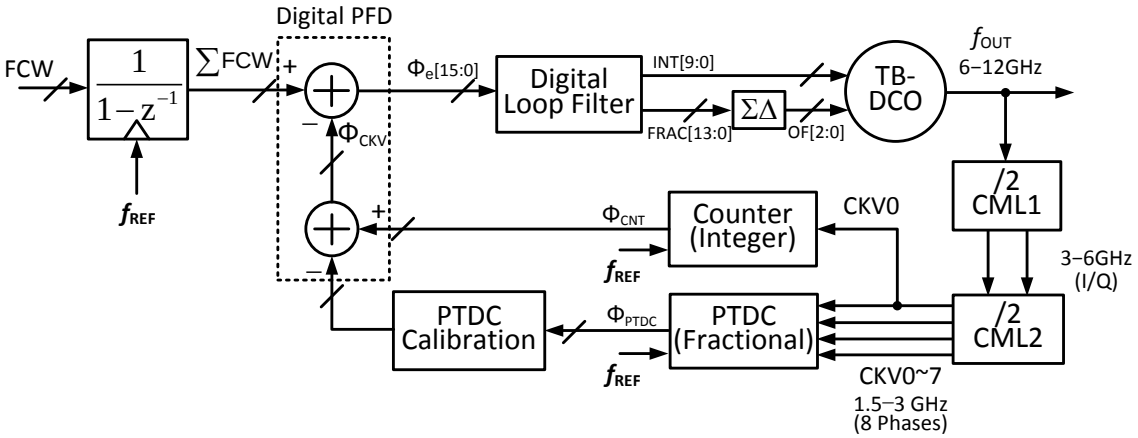


Fig. 4.2 Architecture of the proposed all-digital PLL

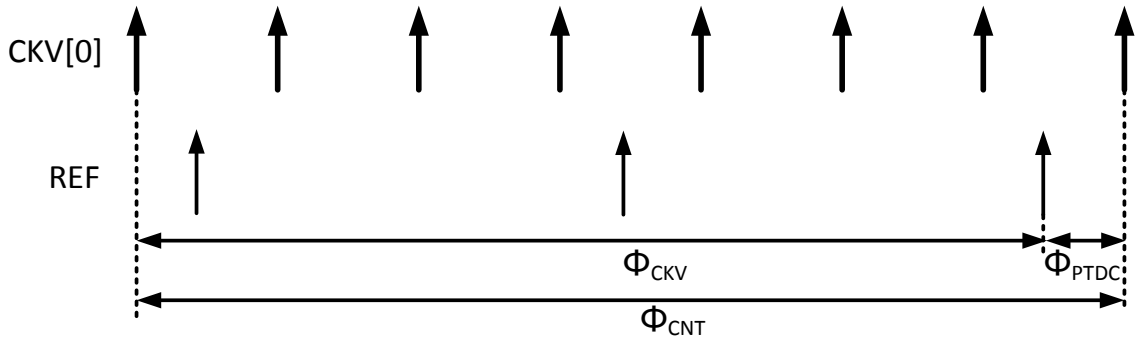


Fig. 4.3 Timing Diagram of the proposed all-digital PLL

4.3 Proposed Phase and Time to Digital Converter (PTDC)

4.3.1 TDC Background

The basic function of the TDC is to measure the time interval between the input edges and convert it to the digital code. Fig. 4.4 shows the classic TDC architecture comprised of a chain of delay elements [6]. It can be seen that the TDC resolution or the quantization error is equal to the delay time of the delay element Δτ. Δτ is limited by the CMOS process, for example, in 65nm CMOS process, the Δτ for a single inverter with minimum transistor size is around 10 ps.

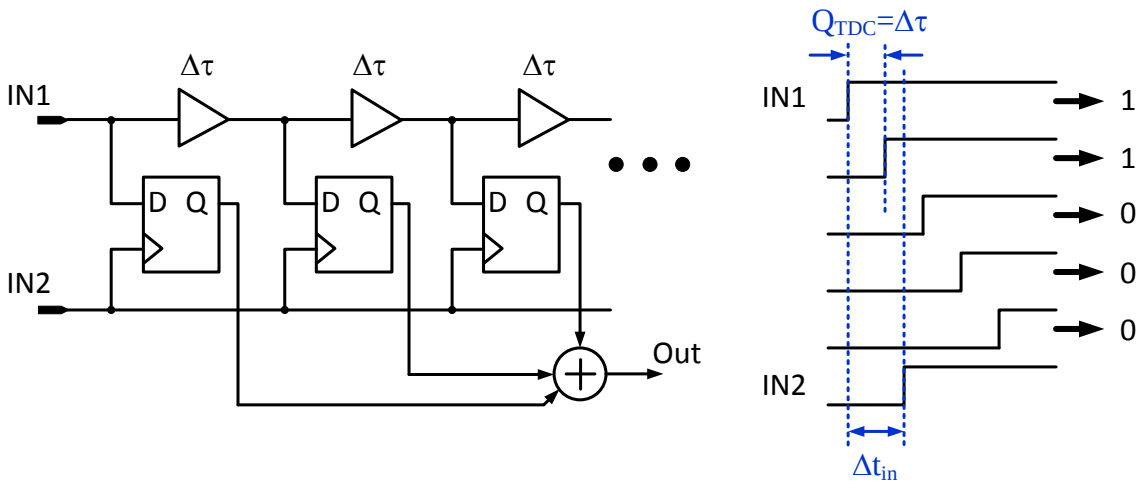


Fig. 4.4 Classical delay-line TDC

To further improve the TDC resolution while still use the same CMOS process, the Veriner delay technique [7] has been widely used to improve the TDC resolution [8][9]. As shown in Fig. 4.5, it can be seen that the TDC resolution $Q_{TDC} = \Delta\tau_1 - \Delta\tau_2$ for the Veriner delay line. Now, the TDC resolution is not limited by the absolute delay time achieved for certain CMOS process, and can be reduced as long as $\Delta\tau_1$ is close to $\Delta\tau_2$. The limitation of the Q_{TDC} now is set by the device mismatch between each delay element.

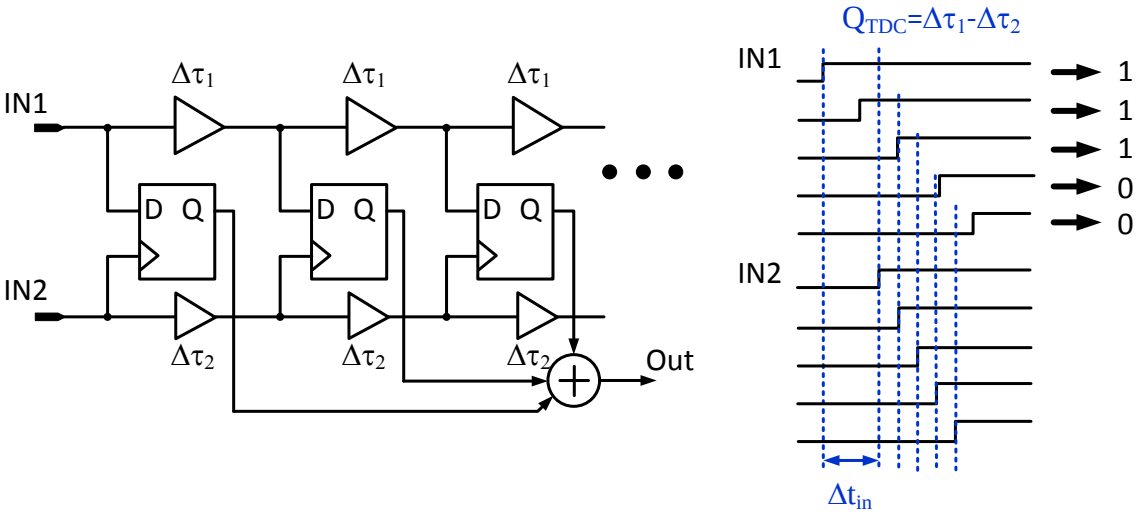


Fig. 4.5 Veriner delay-line TDC

4.3.2 TDC Requirement

The TDC performance is mainly characterized as resolution, input range and linearity. The in-band phase noise of an ADPLL contributed by the TDC quantization noise can be express as following [4]:

$$\mathcal{L} = 4\pi^2 \cdot \frac{Q_{TDC}^2}{12} \cdot \frac{f_{OUT}^2}{f_{REF}} \tag{4.1}$$

where Q_{TDC} is the TDC resolution, f_{REF} and f_{OUT} are the ADPLL reference signal and the ADPLL output frequency, respectively as defined in Fig. 4.1. In this design, the

f_{OUT} is from 6 to 12 GHz. If f_{REF} is 50 MHz, then if we want the in-band phase noise contribution from the TDC to be lower than -98 dBc/Hz, then $Q_{TDC} < 4$ ps is required when f_{OUT} = 12 GHz for the worst case. Besides, TDC with finer resolution can also results in smaller fractional spurs [10].

Together with the TDC resolution, the TDC input range with decides the required number of bits a TDC. In this design, the input range is just $1/f_{OUT}$, which is varies from 333 ps to 666 ps. So a 4 ps TDC resolution requires the TDC to have 8 bits.

The non-linearity of TDC characteristics will also cause fractional spurs. When the TDC resolution is reduced fine enough, the non-linearity will become the dominate source of the fraction spur generation [5]. Besides, it will also cause the phase noise at large offset frequency to be folded into in-band offset frequency, which in turn increases the in-band phase noise level. An effective way to improve the TDC linearity is to reduce the number of bits of the TDC, since less bits indicate small device mismatch in the CMOS process.

For certain input range, TDC resolution and linearity will always be traded-off. If fine TDC resolution is needed, the TDC needs to have more bits, which requires more delay cells and results in poor linearity and large power consumption. So it is worth to explore new TDC architecture to break the resolution and linearity trade-off.

4.3.3 PTDC Architecture

Fig. 4.6 and Fig. 4.7 show the block diagram and the timing diagram of the proposed hybrid PTDC, respectively. The 8-phase input signals CKV[7:0] generated from the frequency division of the DCO output are sent to the phase to digital converter (PDC) and time to digital converter (TDC), respectively.

In the PDC, the inputs CKV[7:0] are sampled by the rising edge of REF to convert the phase difference between REF and CKV[0] to the digital domain. Since the resolution of the PDC is only 3 bits, the TDC is employed here to further achieve fine resolution.

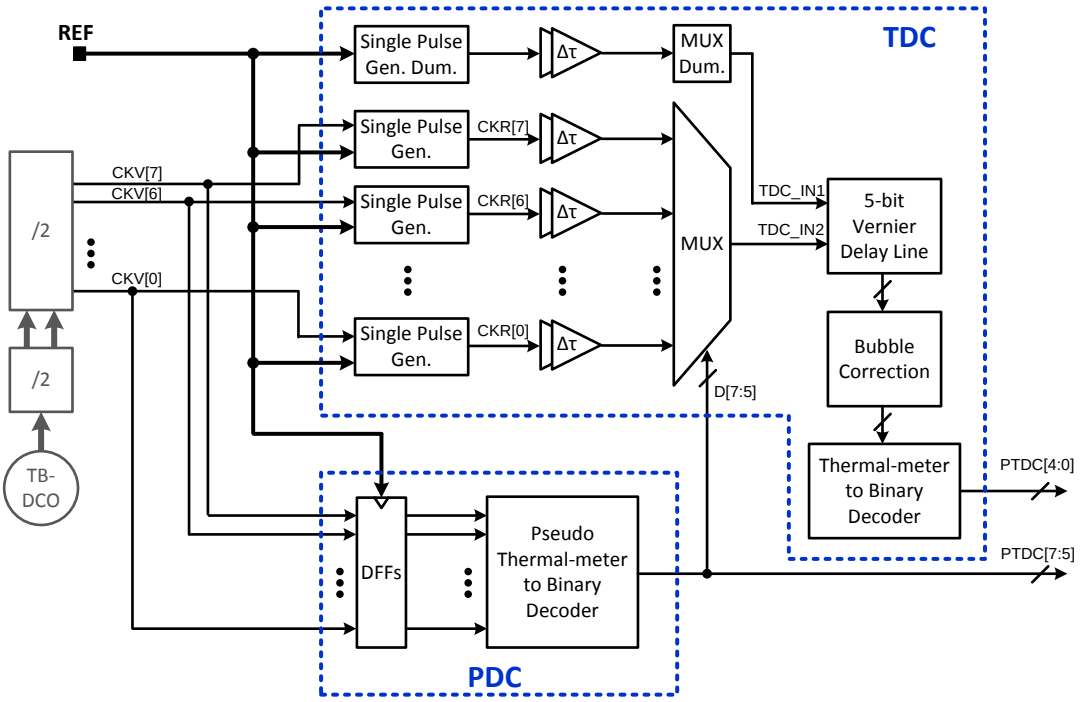


Fig. 4.6 Block diagram of the proposed PTDC

In the TDC, the REF is first sampled by the CKV[7:0] to generated the single pulse signals CKR[7:0]. The CKR only contain the information of a single rising edge comes right after REF. From the Fig. 4.7, it can be seen that the PDC only quantize the time difference Δt_1, so the time residue Δt_2 needs to be sent to the TDC. To determine the time residue Δt_2, the CKR which has the rising edge most close to the RFE needs to be found out. Since the outputs of the PDC after the pseudo thermal-meter to binary decoder already contains this information, the D[7:5] can be used to select the desired CKR[i]. For example, in Fig. 4.7, D[7:5]=3'b101, which indicates that the rising edge of CKR[5] is most close to the rising edge of REF, so the CKR[5] will be selected by a

multiplexer (MUX) and sent to the fine TDC implanted by a 5-bit veriner delay line to convert the time difference between the rising edge of REF. Since the D flip flops (DFFs) and the decoder in the PDC will cause time delay between the PDC inputs and outputs, so a delay $\Delta\tau$ is inserted between CKR[i] and the MUX to guarantee that the selection signals D[7:5] are ready before the rising edge of the desired CKR[i] arrives the MUX. To keep the delay of REF the same as the delay of the desired CKV[i] the same at the vernier delay line inputs, the dummy single pulse generator and MUX are inserted in the REF path.

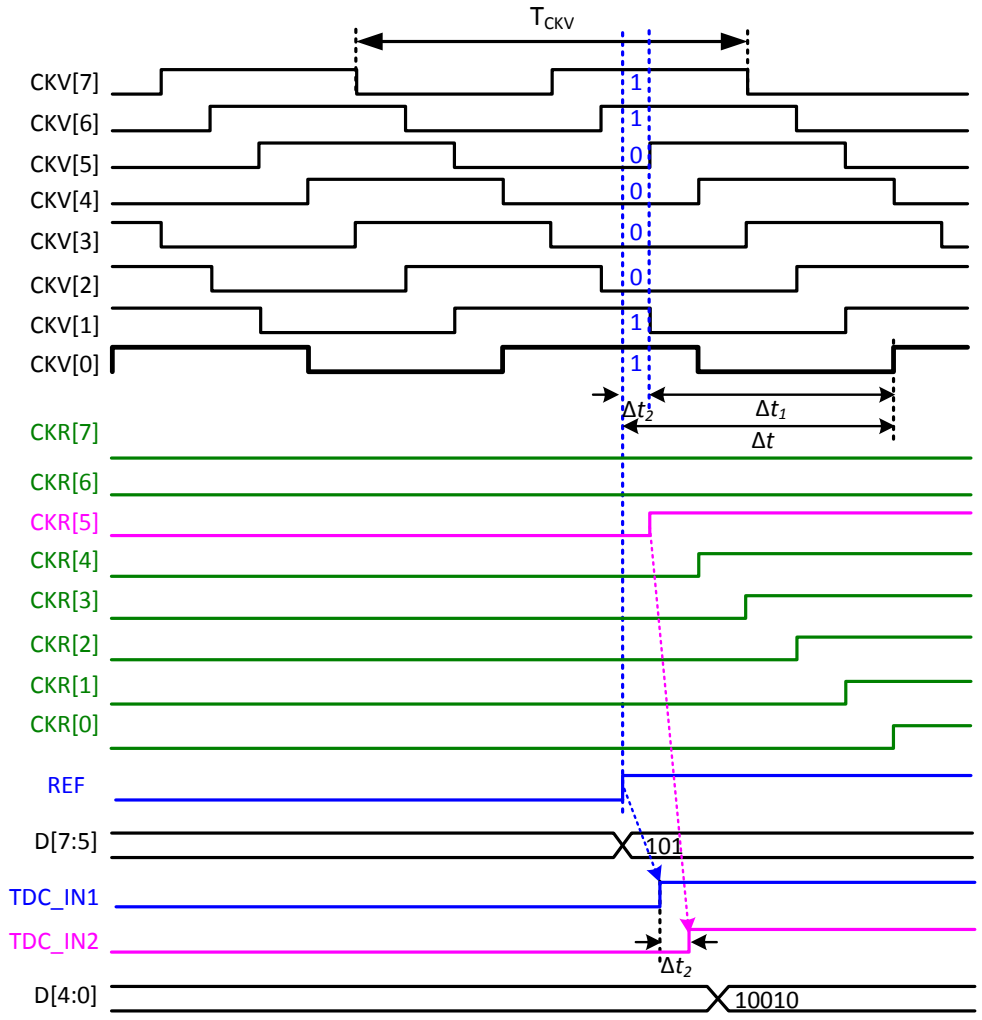


Fig. 4.7 Timing Diagram of the proposed PTDC

The proposed PTDC reduce the input range (Δt_2) of the veriner delay line to only 1/8 of the input period (T_{CKV}), which reduce the total delay cells by 8 times if the resolution is kept the same. As a result, the linearity is improved and power consumption is reduced. In the following sections, the design issues in the PTDC will be discussed.

4.3.4 Single Pulse Generation

Converting the high frequency inputs CKV[7:0] to single pulses CKR[7:0] have two advantages. Firstly, it relaxes the comparison time of the delay line. Even with a comparison time large than T_{CKV}, the delay line output will not be change buy mistake since CKR only has one rising edge at each reference cycle. As a result, no extra logic is needed to hold the delay line outputs. Secondly, it reduces the power consumption greatly since the delay line now operates at the reference frequency instead of the PTDC input frequency (f_{CKV}).

The implementation of the single pulse generator is not trivial. The conventional method by using a DFF suffers from the metastability problem. As shown in Fig. 4.8, if the rising edge of REF is close to the rising edge of CKV[i], then due to the metastability of the DFF [11], the output CKR [i] may delay a random time before transits to the high voltage level. As a result, the timing information contained in the rising edge contained in the CKV[i] would be corrupted after converted to the single pulse CKR[i].

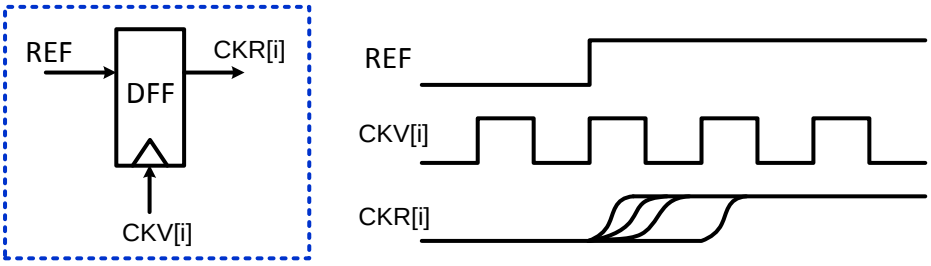
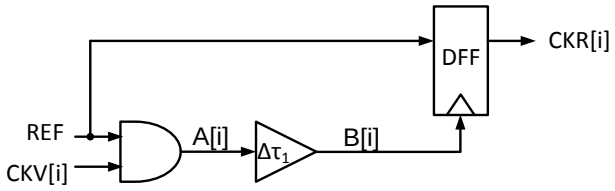
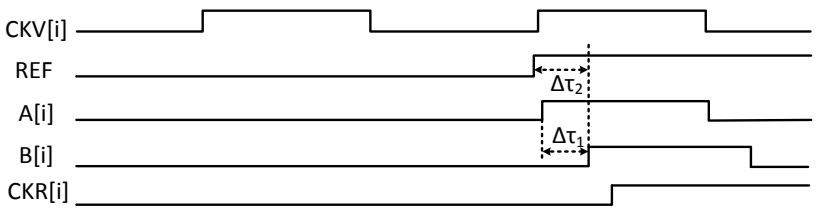


Fig. 4.8 Metastability problem in the DFF method for single pulse generation

To solve this problem, the AND gate based method as shown in Fig. 4.9(a) is used in this design. Since only the CKV with the rising edge after the REF will be selected to pass to the vernier delay line, we just consider the case that the rising edge of CKV[i] is after that of the REF. The REF and CKV[i] are sent to the AND gate to generate the signal A[i]. When REF is high, A[i] follows the CKV[i] and contains the timing information of the CKV[i]. A[i] is then delayed by $\Delta\tau_1$ before being used to sample the REF through a DFF to make sure that the delay $\Delta\tau_2$ from REF to B is longer than the set-up time required by the DFF. By this way, the metastability problem from the DFF is avoided.



(a)



(b)

Fig. 4.9 (a) AND gate based single pulse generation scheme and (b) corresponding timing diagram

4.3.5 Counter and PTDC Interface

To obtain the counter output correctly at each rising edge of the reference clock, the reference clock is usually retimed to sample the counter outputs [12] as shown in Fig. 4.10(a). However, this conventional scheme also suffers from the metastable problem of the DFF. As shown in Fig. 4.10(b), if REF is leading and close to CKV[0], the correct counter output should be fetched after edge 1 of CKV[0]. But due to metastability of the DFF, the rising edge of CKV_R may have chance to delay until edge 2 of CKV[0], which results in a wrong counter output 1 larger than the correct output.

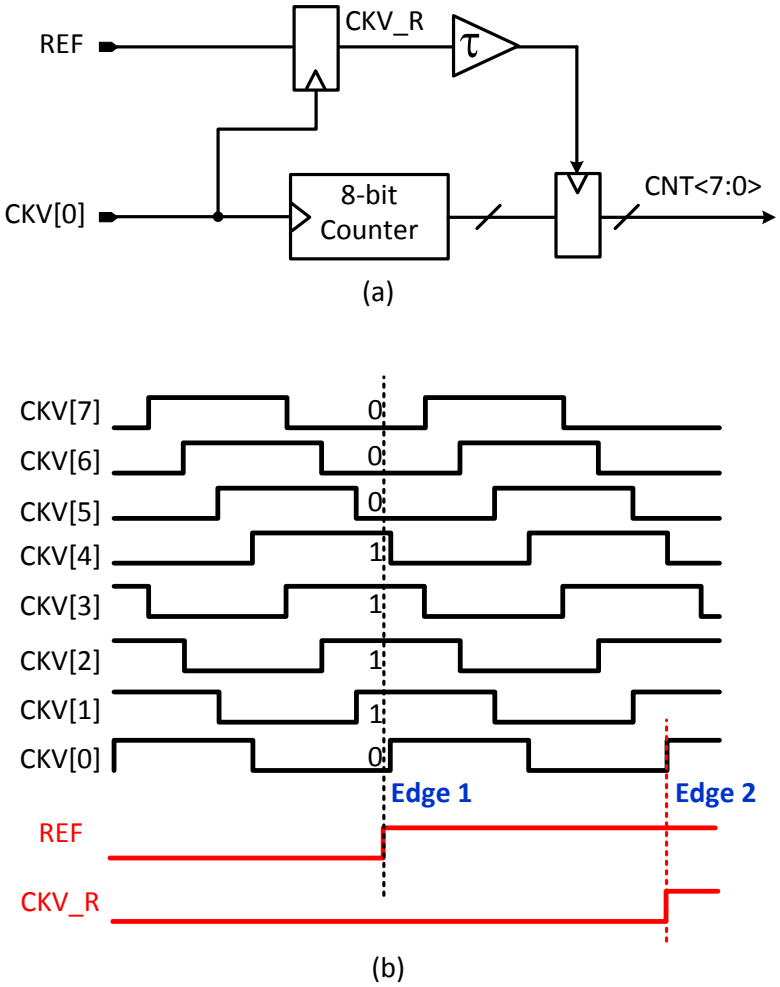
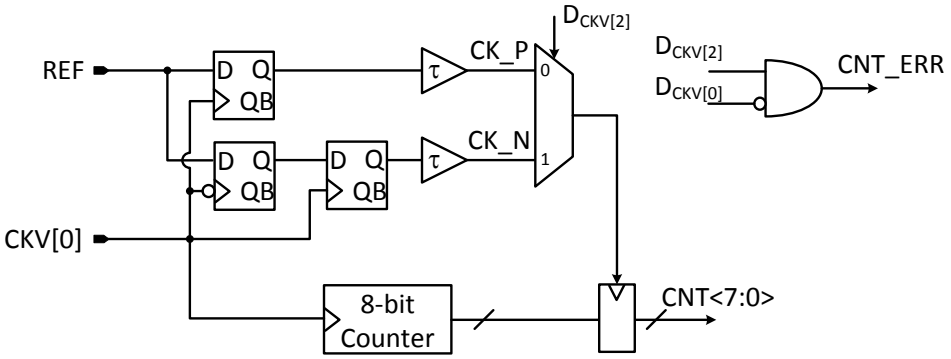


Fig. 4.10 Conventional reference clock retiming scheme: (a) Circuit block diagram, (b) Timing diagram

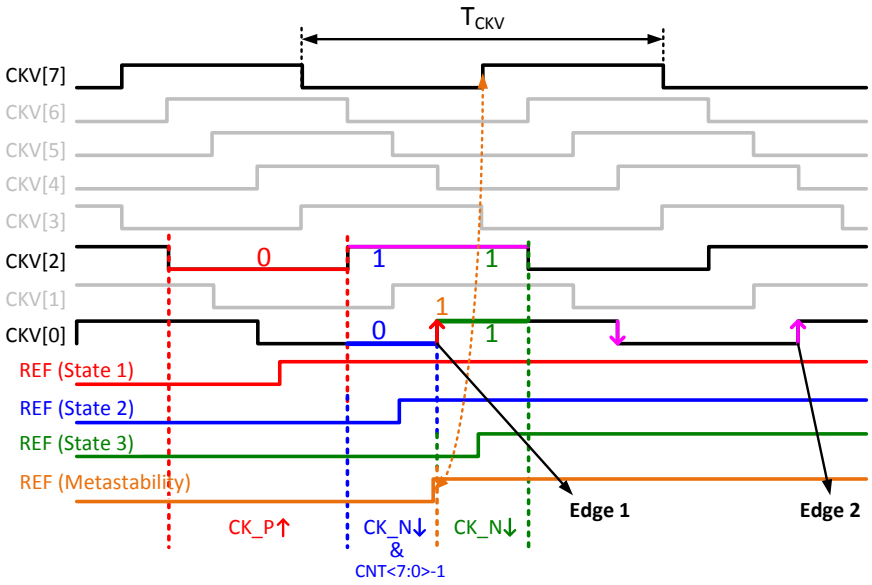
To solve this retiming problem, the new reference clock retiming scheme is proposed to use both the rising edge and falling edge of the CKV[0] as shown in Fig. 4.11(a). Here, CKV[2] is used to select whether the rising edge or the falling edge of the CKV[0] should be employed to retime the reference clock. As shown in Fig. 4.11(b), 4 different state can be discussed to show that the sampled counter outputs are always correct:

1) In state 1, if CKV[2]=0, then the rising edge of CKV[0] is at least TCKV/4 away from the rising edge of REF, so there is no metastable problem.
2) In state 2, if CKV[2]=1 and CKV[0]=0, then the following edge of the CKV[0] will be employed to retime the REF. Since the following edge of CKV[0] is also at least TCKV/4 away from the rising edge of REF, there is still no metastable problem. However, since the counter output is sampled at the edge 2 of the CKV[0] while the PTDC output represents the time interval between the rising edge of REF between the edge 1 of the CKV[0], so the counter output needs to subtract 1 to get the correct output.
3) In state 3, CKV[2]=1 and CKV[0]=1, the situation is almost the same as in state 2. The only difference is now the counter output is sampled at the edge 2 of the CKV[0] and the PTDC output represents the time interval between the rising edge of REF between the edge2 of the CKV[0], so the counter and PTDC outputs are properly aligned and no 1 needs to be subtracted from the counter output.
4) If the PDC output is wrong due to the metastability when sampling the CKV[7:0] by the REF, for example, the rising edge of REF appears just a little bit ahead of edge 1 of CKV[0], but the sampled value is CKV[2]=1 and

CKV[0]=1. Then the counter output the sampled at the edge 2 of the CKV[0] just like in state 3. Since the PTDC output code now already represents the time interval between the rising edge of REF between the edge 2 of the CKV[0], so the counter and PTDC outputs are still properly aligned.



(a)



(b)

Fig. 4.11 Proposed reference clock retiming scheme: (a) Circuit block diagram, (b) Timing diagram

4.3.6 PTDC Calibration Scheme

The PTDC calibration scheme based on a statistical measurement of the fractional phase outputs [10] has been employed to improve the PTDC linearity. As shown in Fig. 4.12, if a histogram of many data samples under uniformly distributed inputs is drawn, the histogram itself represents the actual quantization step sizes of the PTDC. If the PTDC is perfectly linear, then output histogram will also be uniform distributed. So we can set the DCO frequency to a fractional ratio that would generate uniform PTDC outputs and measure the histogram. Base on the measured histogram, a lookup table (LUT) can be used to adding the errors back to the PTDC outputs, which makes the PTDC output after calibration to be uniformly distributed under the uniformly distributed inputs.

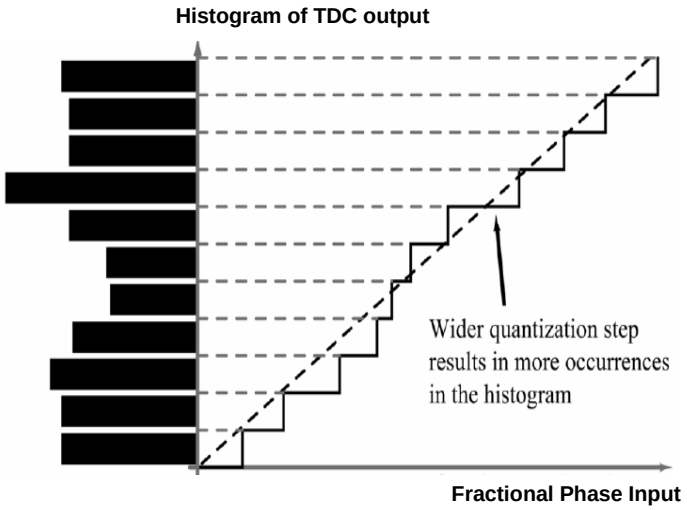


Fig. 4.12 Example of the histogram of the fractional phase detector with PDC nonlinearity [10]

Fig. 4.13 shows the implementation of the PTDC calibration scheme. Here, A(Integer, Fraction) indicates the number of integer bits and fraction bits assigned to each signal line. It is assumed that every signal is in signed representation unless

specified. Since the digital number is represented with fixed-point arithmetic in hardware implementation, the total bit-width is defined by integer bit and fractional-bit. The LUT is mapped to a 352-bit shift register, which can import the errors of the PTDC quantization steps from the statistical measurement.

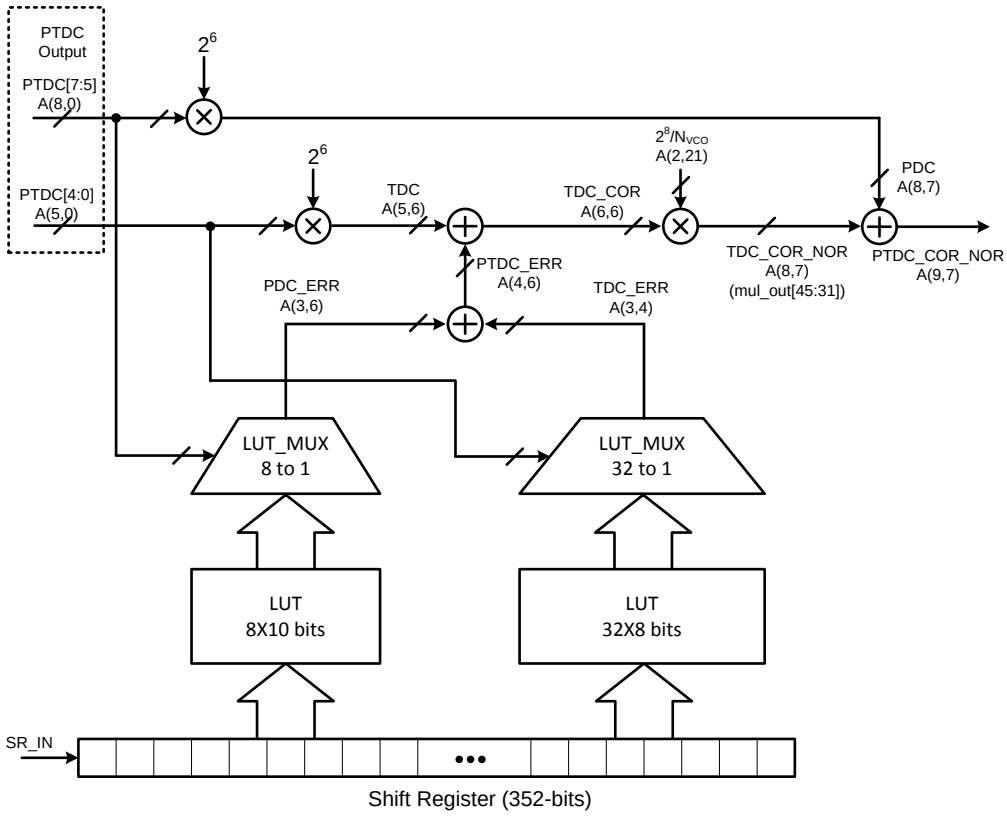


Fig. 4.13 Implementation of the PTDC calibration scheme

4.4 Proposed Triple-Band DCO

The finite step of the DCO frequency will add quantization noise at the DCO output. The phase noise contributed by the quantization noise of the DCO can be expressed as following [13]:

$$\mathcal{L}(\Delta f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \cdot \frac{1}{f_{\mathrm{REF}}} \cdot \left(\sin \mathrm{c} \frac{\Delta f}{f_{\mathrm{REF}}} \right)^2 \tag{4.2}$$

where Δf is the offset frequency from the carrier frequency, f_{REF} is the reference frequency and Δf_{res} is the frequency resolution of the DCO. It can be seen that small Δf_{res} is required to reduce the phase noise contributed by quantization noise of DCO. For example, with the finest frequency resolution of around 15 KHz achieved by using the smallest MOS capacitor size and f_{REF} = 50 MHz, the resulting phase noise would be $\mathcal{L}$ =-125 dBc/Hz at 1MHz offset. This phase noise is even higher than the natural DCO phase noise which is -132 dBc/Hz at 1MHz offset at 1.5 GHz carrier frequency. So dithering of the MOS capacitors with ΣΔ noise shaping is needed to further reduce the quantization noise and push this noise to high offset frequency. The phase noise by using dithering with ΣΔ noise shaping can be expressed as following [13]:

$$\mathcal{L}(\Delta f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \cdot \frac{1}{f_{\text{dth}}} \cdot \left(2 \sin \frac{\pi \Delta f}{f_{\text{dth}}} \right)^{2n} \tag{4.3}$$

where f_{dth} is the sampling frequency for dithering and n is the order of the SD modulator. In this design, third-order ΣΔ modulator is used and $f_{dth} = f_{CKV}/8$.

Fig. 4.14 shows the proposed triple-band DCO based on the triple-band VCO proposed in Chapter 3. Another coil L_3 with the switch varactor bank for digital frequency tuning is added to the switched-transformer between L_1 and L_2. Since L_1 is coupled to both L_2 and L_3, then all the three bands can share the same switch varactor bank. If the coupling coefficient k_{13} and k_{23} between L_1 and L_3 and between L_2 and L_3 are small. then the effective capacitance value will be reduced if transfer from L_3 to L_1 or L_2. Since the DCO resolution is limited by the smallest varactor size available in a certain generation of CMOS process, the DCO resolution is improved by connecting the

varactor with the smallest size to L_3. The switch varactor bank is controlled by the outputs of the digital loop filter INT[9:0] and the ΣΔ modulator OF[2:0], respectively.

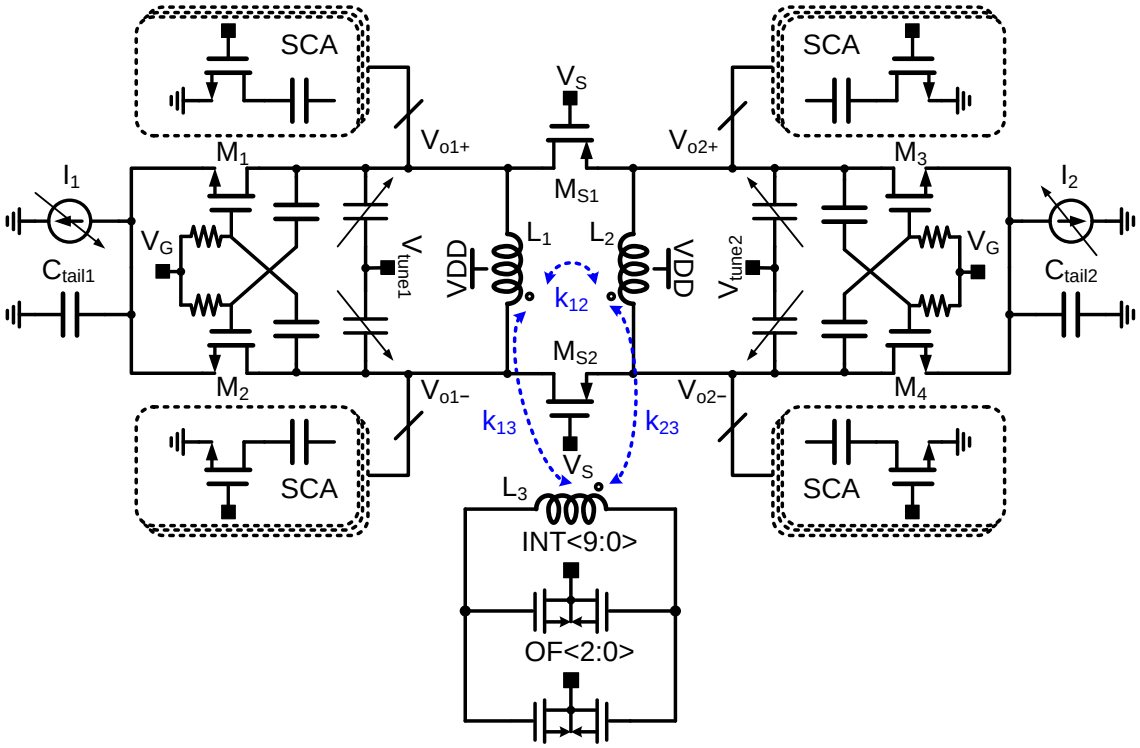


Fig. 4.14 Schematic of the proposed triple-band DCO

4.5 Loop Dynamic and Behavior Simulation

4.5.1 ADPLL model

Fig. 4.15 shows the z-domain model of both the ADPLL architecture with and without feedback divider as shown in Fig. 4.1, respectively. Here, N is the dividsion ratio between the VCO and reference frequency and is equal to the FCW. Since in the architecture II, the phase error ϕ_E at the phase detector output is referred to the VCO period, so the TDC gain is $T_{VCO}/\Delta t_{TDC}$, while in architecture I, the TDC gain in $T_{REF}//\Delta t_{TDC}$ since ϕ_E is referred to the reference clock period. Another thing to be

mentioned is in architecture II, the Δt_{TDC} is the TDC resolution after normalized to the VCO period.

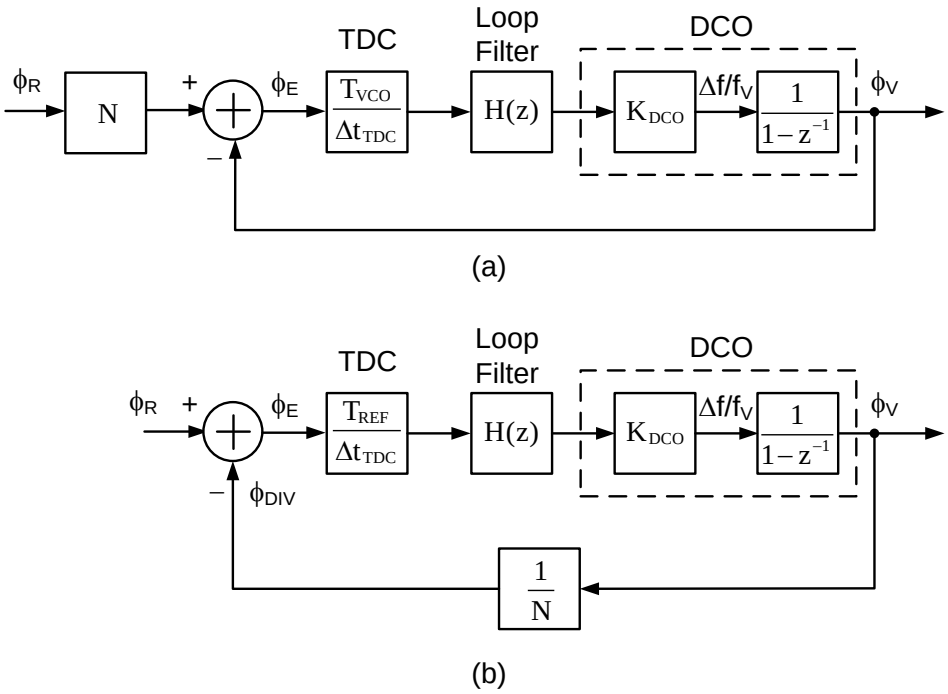


Fig. 4.15 z-domain model of (a) ADPLL architecture II without feedback divider and (b) ADPLL architecture I with feedback divider

So the open loop and close loop phase transfer function of the ADPLL architecture II can be expressed as following according to Fig. 4.15(a):

$$H_{ol\_II}(z) = K_{DCO} \cdot \frac{T_{VCO}}{\Delta t_{TDC}} \cdot \frac{H(z)}{1-z^{-1}} \tag{4.3}$$

$$H_{cl\_II}(z) = \frac{\Phi_V(z)}{\Phi_R(z)} = N\frac{H_{ol\_II}(Z)}{1+H_{ol\_II}(Z)} = \frac{K_{DCO} \cdot \frac{NT_{VCO}}{\Delta t_{TDC}} \cdot \frac{H(z)}{1-z^{-1}}}{1+K_{DCO} \cdot \frac{T_{VCO}}{\Delta t_{TDC}} \cdot \frac{H(z)}{1-z^{-1}}} \tag{4.4}$$

And the open loop and close loop phase transfer function of the ADPLL architecture I can be expressed as following according to Fig. 4.15(b):

$$H_{ol\_I}(z) = K_{DCO} \cdot \frac{T_{REF}}{N\Delta t_{TDC}} \cdot \frac{H(z)}{1-z^{-1}} \tag{4.5}$$

$$H_{cl\_I}(z) = \frac{\Phi_V(z)}{\Phi_R(z)} = \frac{NH_{ol\_I}(Z)}{1+H_{ol\_I}(Z)} = \frac{K_{DCO} \cdot \frac{T_{REF}}{\Delta t_{TDC}} \cdot \frac{H(z)}{1-z^{-1}}}{1+K_{DCO} \cdot \frac{T_{REF}}{N\Delta t_{TDC}} \cdot \frac{H(z)}{1-z^{-1}}} \tag{4.6}$$

From Eqs. (4.4) and (4.6), it can be seen the close loop phase transfer function of architecture I and II are just the same if replace $T_{VCO} = T_{REF}/N$. So either model can be used to calculate the coefficients in the digital loop filter H(z).

Fig. 4.16 shows the ADPLL model for loop filter coefficients calculation. By using the similar method from [14] for the architecture I with feedback divider, the loop filter coefficients for architecture II can be ontained. The discrete-time transfer function can be obtained from the continuous-time loop transfer function expressed as following:

$$A(s) = \frac{T}{\Delta t_{del}} \frac{K_{DCO}}{N} \frac{1}{s} H(z) \tag{4.7}$$

where T is the period of the reference clock, K_{DCO} is the DCO step and N is the division ratio between the DCO output frequency and the reference frequency.

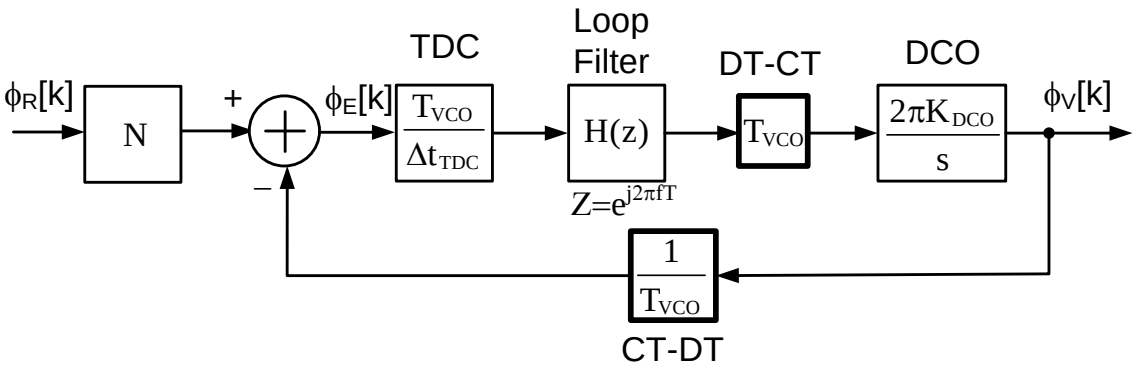


Fig. 4.16 ADPLL model for loop filter coefficients calculation

At low frequencies where |sT|<<1, the first order term of a Talyor series expansion can be used to approximate z^{-1}:

$$z^{-1} = e^{-sT} \approx 1 - sT \tag{4.8}$$

In this design, the 3rd order filter with a parasitic pole (totally 4th order) is employed, then its continuous-time open loop transfer function A(s) is expressed as below:

$$A_{calc}(s) = \frac{K}{s^{Type}} \frac{\left(1+\frac{s}{w_z}\right)}{\left[1+\frac{s}{w_p Q_p}+\left(\frac{s}{w_p}\right)^2\right]} \frac{1}{\left(1+\frac{s}{w_{par}}\right)} \tag{4.9}$$

Given the loop bandwidth and phase margin requirements, the parameters wp, wz, wpar and Qp can be calculated by equations or programs.

Assuming the digital filter is in the following form:

$$H(z) = \frac{K_{LF}}{\left(1-z^{-1}\right)} \frac{\left(1-b_1 z^{-1}\right)}{\left(1-a_1 z^{-1}-a_2 z^{-2}\right)\left(1-a_3 z^{-1}\right)} \tag{4.10}$$

Then put (4.8) into (4.10) and compare the coefficient with (4), the coefficients of the digital filter can be obtained:

$$a_1 = \frac{2+\frac{w_p T}{Q_p}}{1+\frac{w_p T}{Qp}+\left(w_p T\right)^2} \tag{4.11}$$

$$a_2 = -\frac{1}{1+\frac{w_p T}{Qp}+\left(w_p T\right)^2} \tag{4.12}$$

$$a_3 = \frac{1}{1+w_{par} T} \tag{4.13}$$

$$b_1 = \frac{1}{1+w_z T} \tag{4.14}$$

$$K_{LF} = \frac{\Delta t_{TDC}}{K_{DCO}} N \frac{1}{b_1(w_z)} \left(w_p T\right)^2 a_3 w_{par} \left(\frac{1}{1 + \frac{w_p T}{Q_p} + (w_p T)^2} \right) \quad (4.15)$$

4.5.2 Behavior Simulation

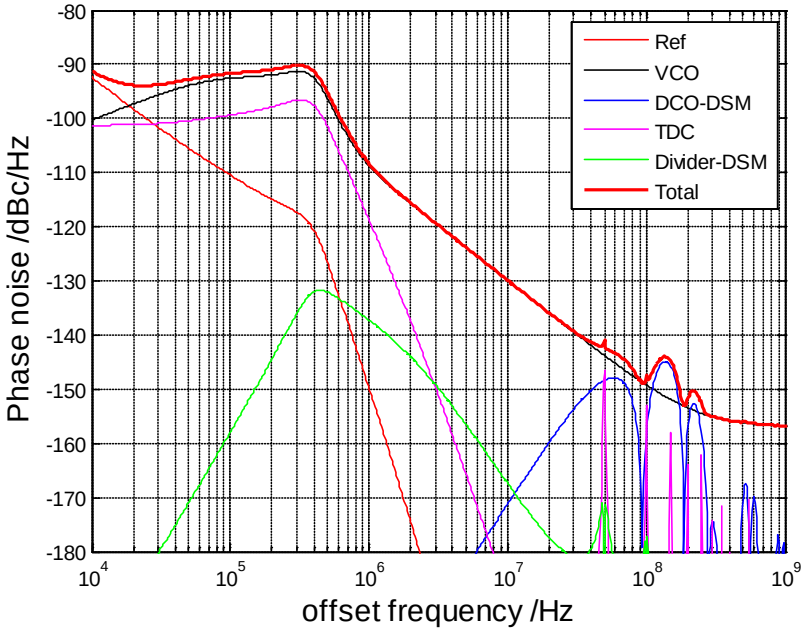
Fig. 4.17 shows the simulation results of the proposed ADPLL output at 12 GHz output with different bandwidth setting. The simulation parameters are listed at Table 4. 1. It can be seen that the choice of the loop bandwidth is the trade-off between the in-band and out-band phase noise.

For small loop bandwidth, the TDC noise at larger offset frequency is well filtered, so the phase noise at 1 MHz offset frequency is just following the DCO phase noise as shown in Fig. 4.17 (a). However, since the DCO noise at small offset frequency is less filtered, it will dominate the in-band phase noise, which decreases the in-band phase noise.

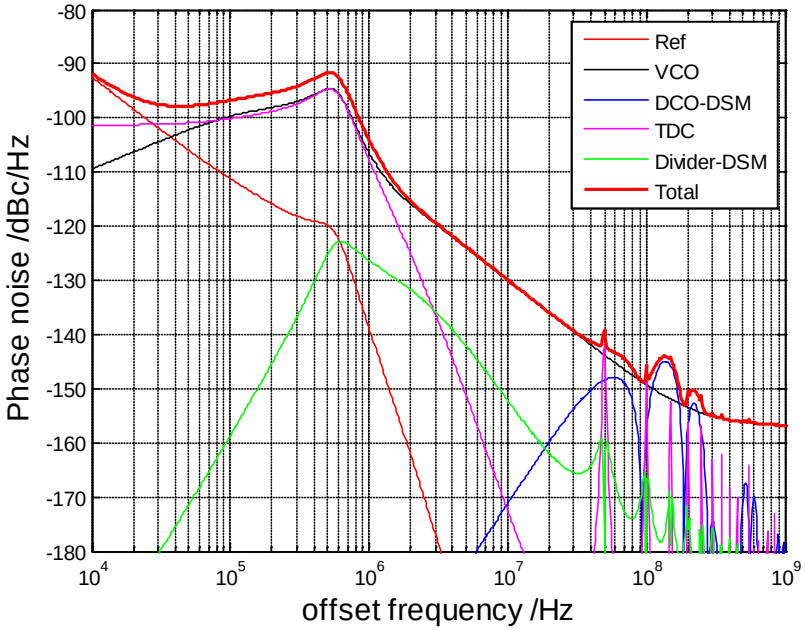
For larger loop bandwidth, the DCO noise at small offset frequency is more attenuated, the in-band phase noise will be improved. However, the TDC out-band noise will increase since it is less filtered. As a result, the phase noise at 1MHz offset frequency increases about 5 dB compared with the DCO phase noise as shown in Fig. 4.17 (b).

Table 4. 1 Parameters used in the behavioral simulation

TDC resolution	2.6 ps
Reference Frequency	50 MHz
DCO gain	400 KHz
DCO ΣΔ dithering frequency	375 MHz
DCO phase noise	-86 dBc/Hz@100kHz offset -110 dBc/Hz @ 1MHz offset
Noise floor	-157 dBc/Hz



(a)



(b)

Fig. 4.17 Simulation results of the ADPLL phase noise at 12 GHz output: (a) 500 kHz loop bandwidth, (b) 800 kHz loop bandwidth.

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Chapter 5

Wide-Band Millimeter-Wave VCO

5.1 Introduction

Recent works on mm-Wave voltage-controlled oscillators (VCOs) are mainly focused on the improvement of their phase noise performance and frequency tuning range [1]-[9]. Since the varactor Q is dominantly low at mm-Wave frequencies, increasing the frequency tuning range by increasing the varactor size would inevitably degrade the tank impedance. To guarantee the oscillation, the size of the negative-gm cell in the VCO would need to be increased, which in turn would increase the parasitic capacitance, degrade the frequency tuning range, and limit the maximum oscillation frequency. The typical tuning range reported by using varactor tuning scheme at mm-Wave frequency is less 10% [1]-[4], which is far from being sufficient for many practical applications when taking into account process variations and inaccurate device modeling.

In RF frequencies, coarse tuning techniques have been proposed to increase the VCO's tuning range. In [10], switched inductors are used for coarse frequency tuning, which increases the frequency tuning range without using a large varactor. However, since the switch is directly connected in series with the inductor, its turn-on resistance severely degrades the quality factor Q of the inductor. In the mm-Wave frequency, since the tank inductance is quite small, increasing the switch size to improve the tank Q is ineffective because the parasitic capacitance would prevent the switch from being

turned off. In [11], switched coupled inductors are used for coarse frequency tuning. Because the effective turn-on resistance of the switch is reduced by the coupling coefficient, the Q degradation is less than that of the switched inductor. However, the total frequency bands created by the switched coupled inductors are limited because the inductor Q drops significantly as the number of switched coupled inductors is increased. In [12]-[15], VCO exploiting high-order LC resonant tanks based on transformers or multi-tapped inductors have been proposed to increase the frequency tuning range while still keeping small chip area. However, the VCOs using high-order LC tank usually suffers from the stability issues, which requires the frequency bands to be separated from each other and result in a discontinuous frequency tuning range.

In this chapter, a novel technique to change the coupling coefficient of a transformer tank in a dual-band VCO to significantly increase its frequency tuning range is presented. By exploiting the three states with different magnetic coupling coefficients created by the proposed switched-triple transformer, the stability problem is eliminated and continuous frequency tuning range is achieved. Based on the derived analytical expressions, the design insights and design procedure of this multi-band MT-VCO are also presented.

This chapter is organized as follows. Section 5.2 describes the working principle of the proposed magnetically-tuned technique and analyzes how to systematically design the switched-tripled-shielded transformer. Section 5.3 presents the proposed MT-VCO, analyzes its performance in terms of the frequency tuning range, tank Q, and phase noise, and summarizes the design flow. Section 5.4 discusses the measurement results, and the conclusion is given in Section 5.5.

5.2 Magnetically Tuning Method

5.2.1 Working Principle of the Magnetically Tuning Method

Fig. 5.1(a) shows the model of the conventional one-port dual-band VCO with a transformer-based LC tank. L_1 and L_2, and C_1 and C_2 denote the inductances and capacitances of the primary coil and the secondary coil, respectively. k is the magnetic coupling coefficient between L_1 and L_2. As illustrated in Fig. 5.2(b), the impedance seen from either coil has two distinct frequency peaks. The VCO tends to oscillate at the peak frequency with higher impedance because it would require less energy.

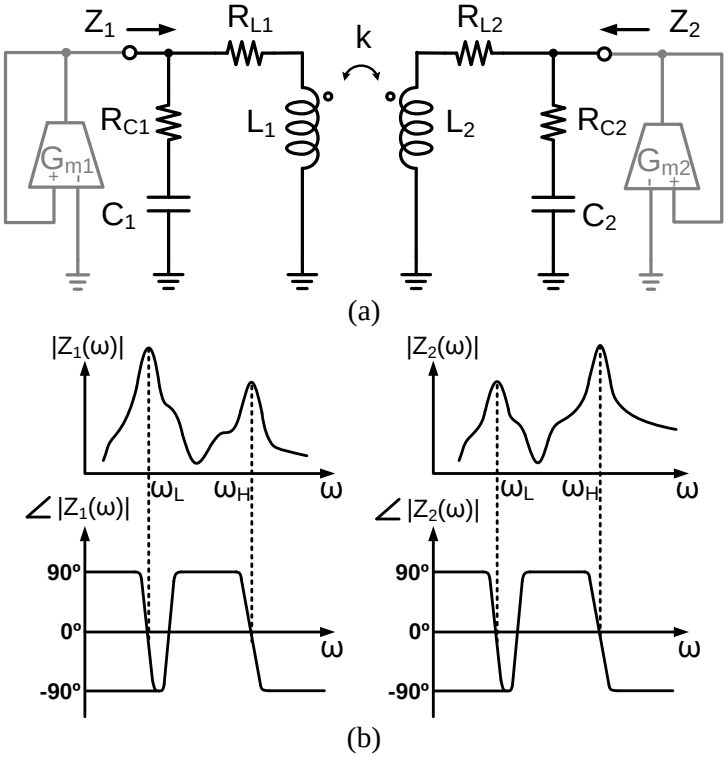


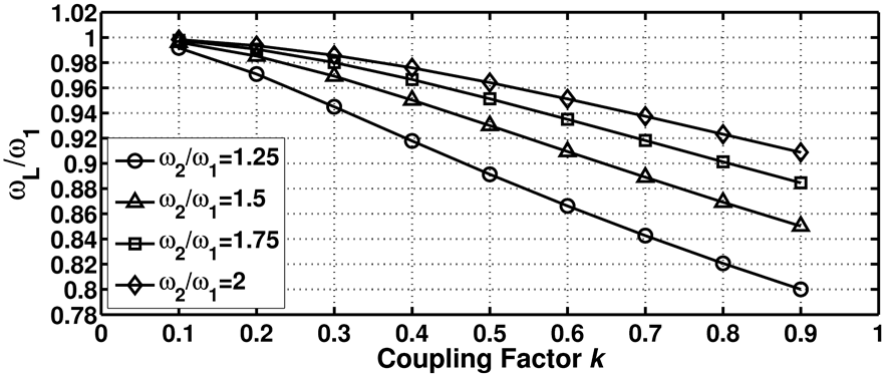
Fig. 5.1 Conventional dual-band VCO: (a) Model, and (b) amplitude and phase of the tank impedance as functions of frequency

If the tank is designed so that $1/\sqrt{L_1C_1} < 1/\sqrt{L_2C_2}$, the oscillation frequencies of the low frequency band (LB) and the high frequency band (HB) can be expressed as [16]:

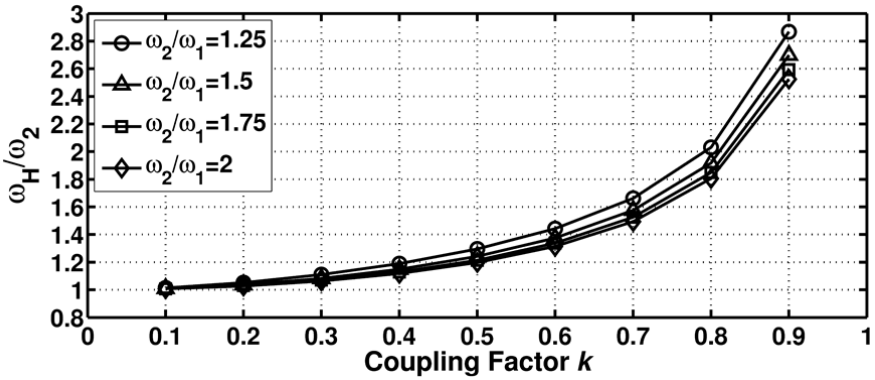
$$\omega_{\mathrm{L}}^2 = \frac{\omega_1^2 + \omega_2^2 - \sqrt{\left(\omega_1^2 - \omega_2^2\right)^2 + 4k^2\omega_1^2\omega_2^2}}{2\left(1-k^2\right)} \tag{5.1a}$$

$$\omega_{\mathrm{H}}^2 = \frac{\omega_1^2 + \omega_2^2 + \sqrt{\left(\omega_1^2 - \omega_2^2\right)^2 + 4k^2\omega_1^2\omega_2^2}}{2\left(1-k^2\right)} \tag{5.1b}$$

where $\omega_1 = 1/\sqrt{L_1C_1}$ and $\omega_2 = 1/\sqrt{L_2C_2}$. From Eqs. (5.1a) and (5.1b), the oscillation frequencies ω_L and ω_H can be tuned by changing ω_1 and ω_2 through changing the capacitor C_1 and C_2, which is the conventional varactor tuning and is limited at mm-Wave frequency as discussed earlier. On the other hand, ω_L and ω_H can also be tuned by changing the magnetic coupling coefficient k assuming that ω_1 and ω_2 are kept constant. Fig. 5.2 plots the relationships between $\omega_{L/H}$ and k for different ω_2/ω_1 ratio, with ω_L and ω_H being normalized to ω_1 and ω_2, respectively. It is clear that ω_H is quite sensitive to the coupling coefficient k. For example, if ω_1 = 60GHz and ω_2 = 75GHz are chosen, ω_H is changed from 77.2 GHz to 85.6 GHz (or 11%) when k increases from 0.15 to 0.35. In other words, tuning the magnetic coupling coefficient k can be employed for coarse frequency tuning.



(a)



(b)

Fig. 5.2 Calculated (a) ω_L and (b) ω_H as functions of the magnetic coupling coefficient k for different $\omega_2 > \omega_1$ ratios

The switched-single-shielded transformer as shown in Fig. 5.3(a) provides a way to change the magnetic coupling coefficient k, where the shielded coil L_A along with a series switch M_A is inserted between the coils L_1 and L_2. Intuitively, when M_A turns on, the current i_1 in L_1 induces a current i_A' in L_A and another current i_2' in L_2, both of which are in the opposite direction with i_1. Since i_A' also in turn induces another current i_2'' in L_2, which tends to cancel i_2', the effective coupling coefficient k_{12} between L_1 and L_2 actually becomes lower as compared with the original transformer without L_A [3]. When M_A turns off, there is no current flowing through L_A, and k_{12} remains almost the same. Consequently, k_{12} can be effectively changed by switching the transistor M_A “on” and “off”.

To obtain the simplified model for analysis, the switch transistor M_A is modeled as an impedance Z_A with $Z_A = R_{on,A}$ when the switch turns on and $Z_A = 1/\omega C_{off,A}$ when the switch turns off, where $R_{on,A}$ and $C_{off,A}$ are the turn-on resistance and turn-off parasitic capacitance of M_A, respectively. By applying the V-I equations to the three coupled coils, the simplified model for the switched-single-shielded transformer as shown in

Fig. 5.4 can be obtained (please refer to the Appendix I for more detail).

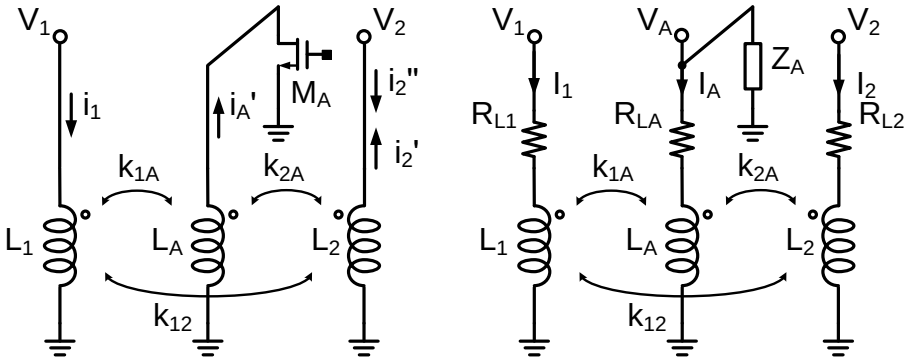


Fig. 5.3 Single-shielded transformer: (a) schematic, and (b) model

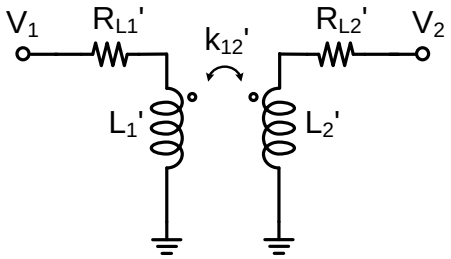


Fig. 5.4 Simplified model of the single-shielded transformer

In the low-k state, the switch M_A is on. Assuming that the quality factor Q_{LA} of the coil L_A is high, and $R_{on,A}$ is small ($R_{LA} + R_{on,A} << \omega L_A$), then the effective inductance L_1', L_2' and the effective magnetic coupling coefficient k_{12}' can be approximated as:

$$L_{1,\text{low-k}}' \approx \left(1-k_{1A}^2\right)L_1 \tag{5.2a}$$

$$L_{2,\text{low-k}}' \approx \left(1-k_{2A}^2\right)L_2 \tag{5.2b}$$

$$k_{12,\text{low-k}}' \approx \left(k_{12}-k_{1A}k_{2A}\right)\sqrt{\frac{L_1L_2}{L_{1,\text{low-k}}'L_{2,\text{low-k}}'}} \tag{5.2c}$$

where k_{1A} and k_{2A} are the magnetic coupling coefficient between L_1 and L_A and between L_2 and L_A, respectively.

In the high-k state, M_A is off. Again, assuming that $Q_{LA} >> 1$, L_1', L_2' and k_{12}' can be

estimated as:

$$L_{1,\text{high-k}}' \approx \left(1+\frac{1}{\omega_A^2/\omega^2-1}k_{1A}^2\right)L_1 \tag{5.3a}$$

$$L_{2,\text{high-k}}' \approx \left(1+\frac{1}{\omega_A^2/\omega^2-1}k_{2A}^2\right)L_2 \tag{5.3b}$$

$$k_{12,\text{high-k}}' \approx \left(k_{12}+\frac{k_{1A}k_{2A}}{\omega_A^2/\omega^2-1}\right)\sqrt{\frac{L_1L_2}{L_{1,\text{high-k}}'L_{2,\text{high-k}}'}} \tag{5.3c}$$

where $\omega_A = 1/\sqrt{L_A C_{off,A}}$. Actually, there are two solutions for $L_{1/2,\text{high-k}}$ in Eqs. (5.3a) and (5.3b), which indicates the dual-resonance characteristic of the transformer tank with capacitor load [11]. Here, the switch size is kept small enough to make sure $\omega_A > \omega$ so that only one resonant mode can occur over the entire frequency tuning range.

From Eqs. (5.2a)-(5.3c), switching on and off of the coil L_A changes not only the coupling coefficient k_{12}' but also the effective inductance of L_1' and L_2', which makes the change of the magnetic coupling coefficient $\Delta k_{12}' = k_{12,\text{high-k}}' - k_{12,\text{low-k}}'$ less significant. Moreover, the differences between $L_{1/2,\text{low-k}}'$ and $L_{1/2,\text{high-k}}'$ also imply that the earlier assumption of constant ω_1 and ω_2 with k_{12} is not quite valid. Furthermore, from Eq. (5.1b), the large drop of ω_1 and ω_2 would decrease ω_H even when k_{12} increases. As such, in order to increase the frequency tuning range, it is highly desirable to keep L_1' and L_2' constant when the switch M_A is turned on and off.

5.2.2 Analysis of the Proposed Switched-Triple-Shielded Transformer

A switched-triple-shielded transformer is proposed to keep the effective inductance L_1' and L_2' constant when M_A turns on and off, as shown in Fig. 5.5(a). In the switched-triple-shielded transformer, two extra coils L_B and L_C with the switches M_B and M_C are added to the left and right sides of L_1 and L_2, respectively. By replacing switches M_A,

M_B and M_C with the impedances Z_A, Z_B and Z_C as shown in Fig. 5.5(b), the simplified model for the switched-triple-shielded transformer as shown in Fig. 5.4 can be derived (again, please refer to the Appendix I for more detail). Although the topology is the same as that of the switched-single-shielded transformer, the expressions for the parameters L_1', L_2', R_1', R_2', and k_{12}' are quite different.

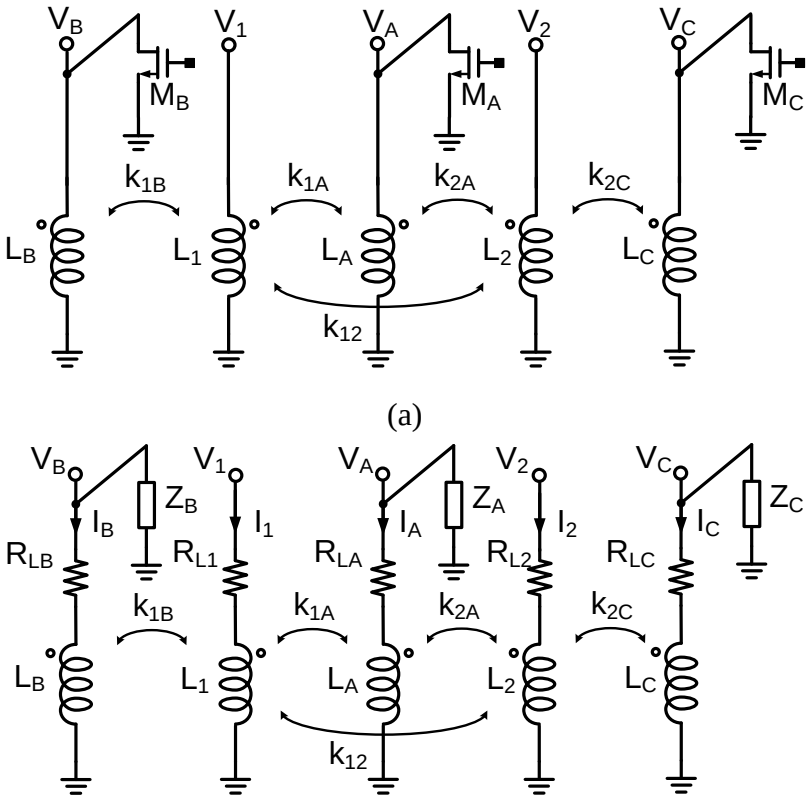


Fig. 5.5 The proposed switched-triple-shielded transformer: (a) schematic, and (b) model

In the low-k state, M_B and M_C are off while M_A is on, and with the assumption of high Q for all the inductors and the turn-on resistance of all the switches are small, the effective parameters L_1', L_2', R_{L1}', R_{L2}', and k_{12}' can be approximated as:

$$L_{1,\text{low-k}}{}' \approx \left[1 - k_{1A}^2 + \frac{1}{\omega_B^2/\omega^2 - 1} k_{1B}^2\right] L_1 \tag{5.4a}$$

$$L_{2,\text{low-k}}{}' \approx \left[1-k_{2A}^2+\frac{1}{\omega_C^2/\omega^2-1}k_{2C}^2\right]L_2 \tag{5.4b}$$

$$R_{\text{L1,low-k}}{}' \approx R_{L1}+\frac{L_1}{L_A}k_{1A}^2\left(R_{LA}+R_{\text{on,A}}\right)+\frac{1}{\left(\omega_B^2/\omega^2-1\right)^2}\frac{L_1}{L_B}k_{1B}^2R_{LB} \tag{5.4c}$$

$$R_{\text{L2,low-k}}{}' \approx R_{L2}+\frac{L_2}{L_A}k_{2A}^2\left(R_{LA}+R_{\text{on,A}}\right)+\frac{1}{\left(\omega_C^2/\omega^2-1\right)^2}\frac{L_2}{L_C}k_{2C}^2R_{LC} \tag{5.4d}$$

$$k_{12,\text{low-k}}{}' \approx \left(k_{12}-k_{1A}k_{2A}\right)\sqrt{\frac{L_1L_2}{L_{1,\text{low-k}}{}'L_{2,\text{low-k}}{}'}} \tag{5.4e}$$

where $\omega_B = 1/\sqrt{L_B C_{\text{off,B}}}$, $\omega_C = 1/\sqrt{L_C C_{\text{off,C}}}$, $\omega_{B/C} > \omega$, k_{1B} and k_{2C} are the magnetic coupling coefficient between L_1 and L_B, and between L_2 and L_C, respectively,.

In the high-k state, M_B and M_C are on while M_A is off. Again with the assumption that all the coils have high Q and the turn-on resistance of all the switches are small, the effective parameters L_1', L_2', R_{L1}', R_{L2}' and k_{12}' can be estimated as:

$$L_{1,\text{high-k}}{}' \approx \left[1+\frac{1}{\omega_A^2/\omega^2-1}k_{1A}^2-k_{1B}^2\right]L_1 \tag{5.5a}$$

$$L_{2,\text{high-k}}{}' \approx \left[1+\frac{1}{\omega_A^2/\omega^2-1}k_{2A}^2-k_{2C}^2\right]L_2 \tag{5.5b}$$

$$R_{\text{L1,high-k}}{}' \approx R_{L1}+\frac{1}{\left(\omega_A^2/\omega^2-1\right)^2}\frac{L_1}{L_A}k_{1A}^2R_{LA}+\frac{L_1}{L_B}k_{1B}^2\left(R_{LB}+R_{\text{on,B}}\right) \tag{5.5c}$$

$$R_{\text{L2,high-k}}{}' \approx R_{L2}+\frac{1}{\left(\omega_A^2/\omega^2-1\right)^2}\frac{L_2}{L_A}k_{2A}^2R_{LA}+\frac{L_2}{L_C}k_{2C}^2\left(R_{LC}+R_{\text{on,C}}\right) \tag{5.5d}$$

$$k_{12,\text{high-k}}{}' \approx \left(k_{12}+\frac{k_{1A}k_{2A}}{\omega_A^2/\omega^2-1}\right)\sqrt{\frac{L_1L_2}{L_{1,\text{high-k}}{}'L_{2,\text{high-k}}{}'}} \tag{5.5e}$$

where $\omega_A = 1/\sqrt{L_A C_{\text{off,A}}}$ and $\omega_A > \omega$.

In both the low-k and high-k states, one of the two coils adjacent to L_1 or L_2 is always switched on while the other is switched off. Consequently, it is possible to design the coupling coefficients k_{1A}, k_{1B}, k_{2A} and k_{2C} and the switch sizes to keep $L_{1,low\text{-}k}' = L_{1,high\text{-}k}'$ and $L_{2,low\text{-}k}' = L_{2,high\text{-}k}'$. By replacing $L'_{1,on}$, $L'_{1,off}$, $L'_{2,on}$ and $L'_{2,off}$ in Eqs. (5.4a), (5.5a), (5.4b) and (5.5b), the following conditions can be obtained:

$$\frac{k_{1A}^2}{k_{1B}^2} = \frac{1-\omega^2/\omega_A^2}{1-\omega^2/\omega_B^2} \tag{5.6a}$$

$$\frac{k_{2A}^2}{k_{2C}^2} = \frac{1-\omega^2/\omega_A^2}{1-\omega^2/\omega_C^2} \tag{5.6b}$$

By making $k_{1A} = k_{1B}$, $k_{2A} = k_{2C}$ and $\omega_A = \omega_B = \omega_C$, Eqs. (5.6a) and (5.6b) can be satisfied even when the frequency ω changes. When $L_{1,low\text{-}k}' = L_{1,high\text{-}k}'$ and $L_{2,low\text{-}k}' = L_{2,high\text{-}k}'$, the effective change of the coupling coefficient $\Delta k_{12}' = k_{12,high\text{-}k}' - k_{12,low\text{-}k}'$ can be expressed below:

$$\Delta k_{12}' = 1 \Big/ \sqrt{\left(\frac{\alpha}{k_{1A}}+1\right)\left(\frac{\alpha}{k_{2A}}+1\right)} \tag{5.7}$$

where $\alpha = \left(2-\omega_A^2/\omega^2\right)\Big/\left(\omega_A^2/\omega^2-1\right)$.

Interestingly, an additional state can also be exploited to further increase the frequency tuning range and relieve the stability problem by simultaneously turning on all the three switches M_A, M_B, and M_C. In this low-inductance (low-L) state, again with high-Q and small turn-on resistance assumption, the effective parameters L_1', L_2', R_{L1}', R_{L2}' and k_{12}' can be approximated as:

$$L'_{1,low\text{-}L} \approx \left[1-k_{1A}^2-k_{1B}^2\right]L_1 \tag{5.8a}$$

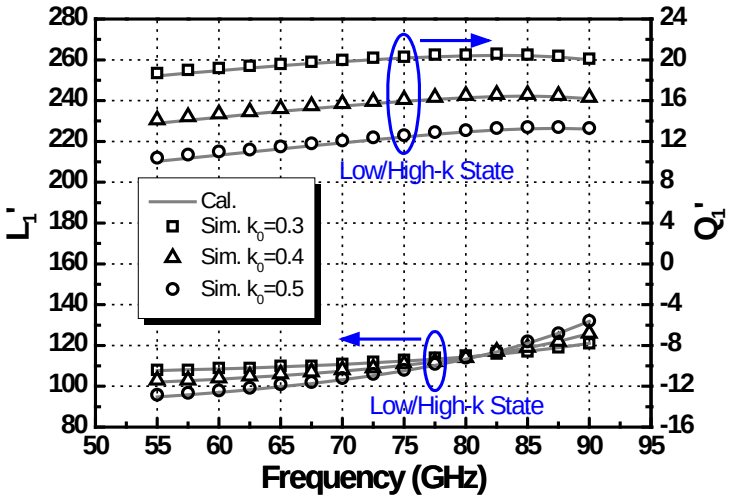
$$L'_{2,low\text{-}L} \approx \left[1-k_{2A}^2-k_{2C}^2\right]L_2 \tag{5.8b}$$

$$R'_{\text{L1,low-L}} \approx R_{\text{L1}} + \frac{L_1}{L_{\text{A}}} k_{1\text{A}}^2 \left(R_{\text{LA}} + R_{\text{on,A}} \right) + \frac{L_1}{L_{\text{B}}} k_{1\text{B}}^2 \left(R_{\text{LB}} + R_{\text{on,B}} \right) \tag{5.8c}$$

$$R'_{\text{L2,low-L}} \approx R_{\text{L2}} + \frac{L_2}{L_{\text{A}}} k_{2\text{A}}^2 \left(R_{\text{LA}} + R_{\text{on,A}} \right) + \frac{L_2}{L_{\text{C}}} k_{2\text{C}}^2 \left(R_{\text{LC}} + R_{\text{on,C}} \right) \tag{5.8d}$$

$$k'_{12,\text{low-L}} \approx \left(k_{12} - k_{1\text{A}} k_{2\text{A}} \right) \sqrt{\frac{L_1 L_2}{L'_{1,\text{low-L}} L'_{2,\text{low-L}}}} \tag{5.8e}$$

Fig. 5.6 compares the calculated parameters for both the low-k and high-k states with the simulated results using the model shown in Fig. 5.5(b), where L_1 = 115 pH, L_2 = 66 pH, L_A = 86 pH, L_B = 150 pH, L_C = 60 pH and k_{12} = 0.3. For simplicity, the Q of each coil is assumed to be constant at 30 as the frequency is changed. To guarantee $L_{1/2,\text{low-k}}' = L_{1/2,\text{high-k}}'$, the condition $k_{1A} = k_{1B} = k_{2A} = k_{2C} = k_0$ is kept, and the switch sizes are designed to keep $\omega_A = \omega_B = \omega_C = \omega_0 = 115$ GHz. The effective parameters are plotted with different k_0 values. From both Fig. 5.6(c) and Eq. (5.7), larger k_0 results in larger $\Delta k_{12}'$. However, larger k_0 would also increase the loss from the shielded coils, which would increase $R_{\text{L1/L2, low-k}}'$ and $R_{\text{L1/L2, high-k}}'$ and degrade Q_{L1}' and Q_{L2}'. So the choice of k_0 is the trade-off between the change of magnetic coupling coefficient $\Delta k_{12}'$ and the quality factors Q_{L1}' and Q_{L2}' of the effective inductances.



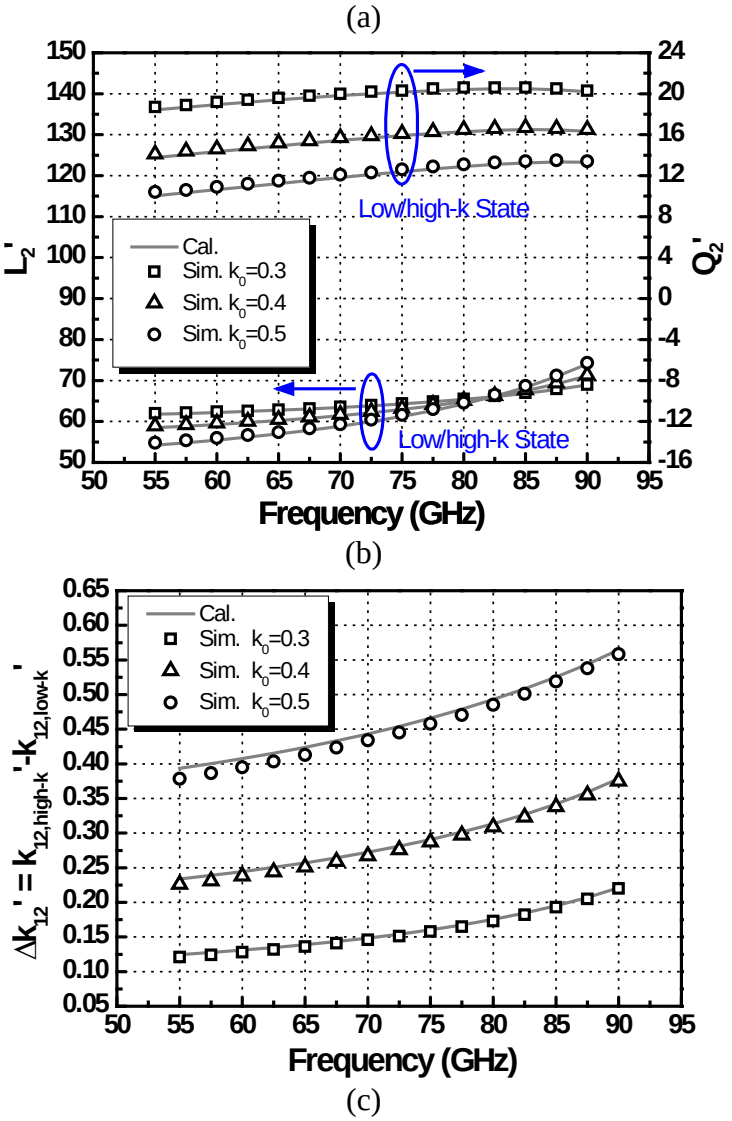
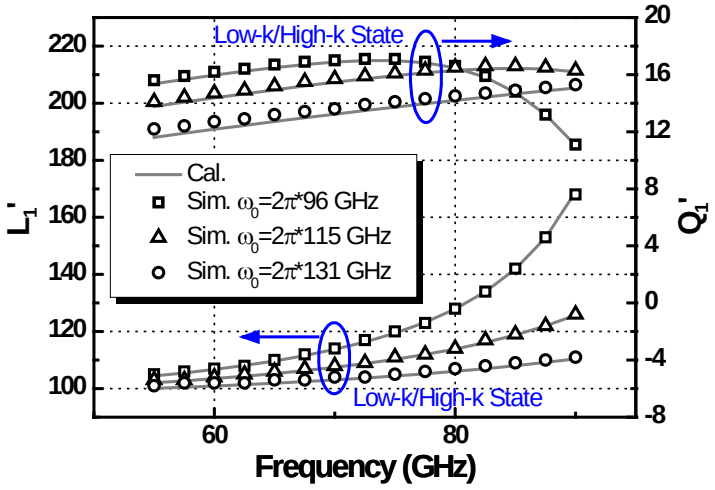


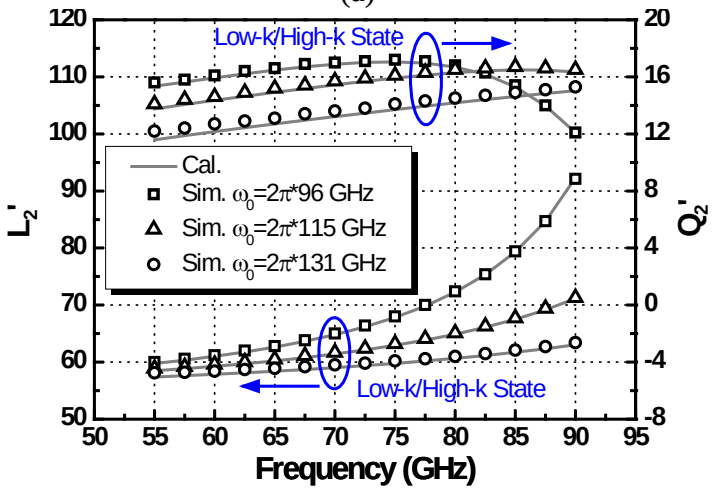
Fig. 5.6 Calculated and simulated values: (a) L_1' and Q_1', (b) L_2' and Q_2', (c) Δk_{12}' for different k_0 ($\omega_A = \omega_B = \omega_C = \omega_0 = 115$GHz)

Fig. 5.7 plots the calculated and simulated effective parameters by using the same L_1, L_2, L_A, L_B, L_C and k_{12} values as used in Fig. 6. Here $k_{1A} = k_{1B} = k_{2A} = k_{2C} = 0.4$ is kept and the switch sizes of M_A, M_B and M_C are changed to obtain different ω_0 values. The turn-on resistor R_A, R_B and R_C are also scaled with the switch sizes. It can be seen that small ω_0 results in better Q_{L1}' and Q_{L2}' when the operating frequency ω is much smaller than ω_0 because the loss of the effective inductances is dominant by the turn-on resistances of the switches, which could be

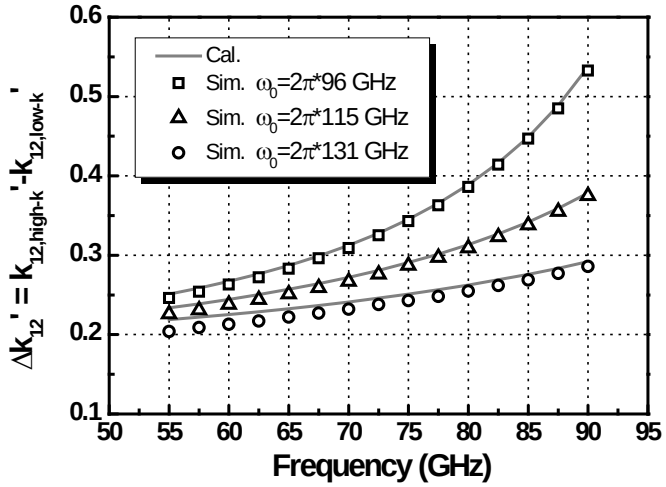
reduced with large switch sizes or smaller ω_0. However, when ω approaches ω_0, Q_{L1}' and Q_{L2}' would start to drop quickly because the series resistance in the shielded coils with the switches being off would dominate the total loss of the effective inductances. As a results, an optimal ω_0 exists for maximizing Q_{L1}' and Q_{L2}' in the desired operating frequency range.



(a)



(b)



(c)

Fig. 5.7 Calculated and simulated values: (a) L_1' and Q_1', (b) L_2' and Q_2', (c) Δk_{12}' for different ω_0 ($k_{1A} = k_{1B} = k_{2A} = k_{2C} = k_0 = 0.4$)

5.3 Design and Analysis of the Proposed Magnetically-Tuned VCO

Fig. 5.8 shows the schematic of the proposed MT-VCO. The switched-triple-shielded transformer described in Section 5.2 is used for coarse frequency tuning while an AMOS varactor array (C_{V2}) consisted of 2-bit digitally-controlled binary-weighted varactors and a varactor (C_{V1}) with an analog control voltage is employed for fine frequency tuning. The PMOS current tails are used to bias the gates of varactors at around 0.8 V with 1.2 V supply voltage to increase the capacitance tuning range of the varactors and thus the frequency tuning range of the MT-VCO.

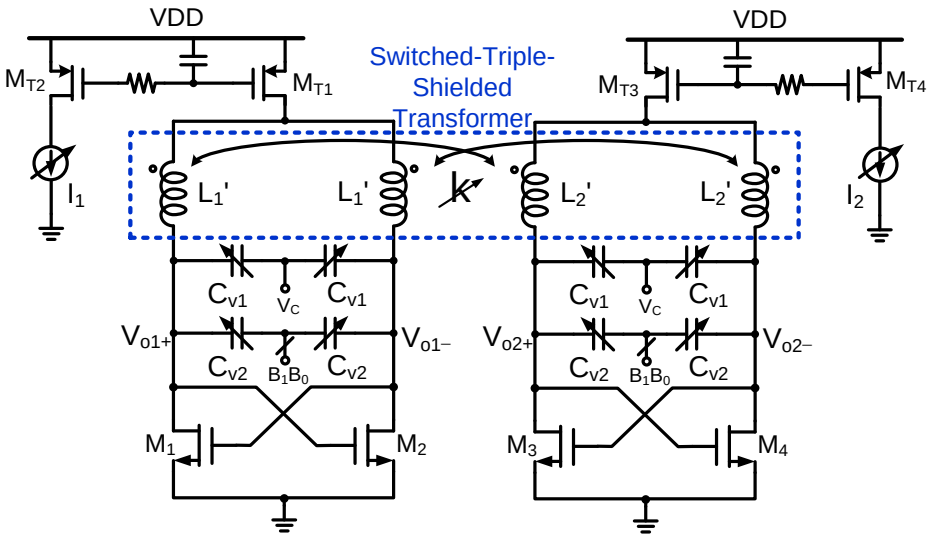


Fig. 5.8 Schematic of the proposed MT-VCO

Since the topology of the proposed MT-VCO is exactly the same as the conventional one-port dual-band oscillator with different designed parameters in the three states, the model shown in Fig. 5.1(a) can also be applied to it, and the VCO design parameters can be obtained as follows by simply using the results from [16] with appropriate expressions for the transformer's parameters L_1', L_2', R_{L1}', R_{L2}' and k_{12}' as derived in Section 5.2.

5.3.1 Frequency Tuning Range

By replacing ω_1, ω_2 and k with $\omega_1'=1/\sqrt{L_1'C_1'}$, $\omega_2'=1/\sqrt{L_2'C_2'}$, and k_{12}', the oscillation frequency of ω_L' and ω_H' for the proposed MT-VCO can still be expressed by Eqs. (5.1a) and (5.1b). Since large $\Delta\omega_H'$ between the low-k and high-k states requires large $\Delta k_{12}'$, large k_0 is desired for larger coarse tuning range. Moreover, from Fig. 5.7(b), when ω approaches ω_0, L_2' starts to increase quickly with frequency, which would in turn decrease ω_2' and limit the maximum achievable ω_H'. As a result, the maximum value of ω_H' can be further extended by increasing ω_0.

The one-port dual-band VCO will suffer from the stability problem [16]. If the amplitude of the two peak impedance at frequency ω_L' and ω_H' shown in Fig. 1(b) are close to each other, then the oscillator could jump from one desired equilibrium oscillation frequency to the other with some disturbance. So the difference between the two peak impedances must be kept large enough to make sure the oscillator only operating at the wanted frequency, which can be achieved by either separating ω_L' and ω_H' far away or reducing the k_{12}'. Fig. 5.9 shows the arrangement of the low frequency band and high frequency band in all the three states. The frequency bands of the low-k state are placed between the frequency bands of the high-k state to separate $\omega_{L,high\text{-}k}'$ and $\omega_{H,high\text{-}k}'$. Moreover, from Eqs. (5.8a) and (8b), because the inductance in the low-L state is smaller than that in both the low-k and high-k states, $\omega_{L,low\text{-}k}'$ and $\omega_{H,low\text{-}k}'$ can be further separated by placing the low frequency band of the additional low-L state between the two frequency bands of the low-k state. Consequently, the proposed MT-VCO can achieve a continuous ultra-wide frequency tuning range without a stability problem. In addition, the high frequency band of the low-L state can be employed to further increase the maximum oscillation frequency.

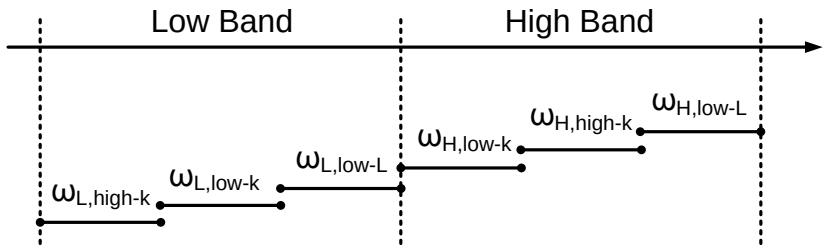


Fig. 5.9 Allocation of the 3 states for the two frequency bands

5.3.2 TankQ

By assuming that $Q_{L1}' = Q_{L2}' = Q_L'$, $Q_{C1}' = Q_{C2}' = Q_C'$ and $L_1'/L_2' = C_1'/C_2'$, the tank Q of both the primary coil (Q_{tank1}') and the secondary coil (Q_{tank2}') can be estimated as [16]:

$$\frac{1}{Q_{tank1}'(\omega_L')} = \frac{\left(n^2 D_1^2 - 1\right) - k_{12}'^2}{\left(n^2 D_1^2 - 1\right) + k_{12}'^2}\frac{1}{Q_L'} + \frac{1}{Q_C'} \tag{5.9a}$$

$$\frac{1}{Q_{tank2}'(\omega_H')} = \frac{\left(1 - D_2^2/n^2\right) + k_{12}'^2}{\left(1 - D_2^2/n^2\right) - k_{12}'^2}\frac{1}{Q_L'} + \frac{1}{Q_C'} \tag{5.9b}$$

where $D_1 = \omega_1'^2/\omega^2$, $D_2 = \omega_2'^2/\omega^2$, and $n = \omega_2'/\omega_1'$. Compared with the second-order LC tank with the same Q_L' and Q_C', the contribution of Q_C' to the fourth-order LC tank's Q is the same, so whether the tank Q of the fourth-order LC tank is enhanced or degraded would mainly depend on the quality factor Q_L' of the effective inductances in the switched-triple-shielded transformer derived in Section 5.2. By assuming $Q_L = 30$, $Q_C = 6$ at around 60 GHz, the Q of the second-order tank is calculated to be 5. By using ω_1' = 60 GHz, ω_2' = 75 GHz, k_{12}' = 0.15/0.35, and assuming that Q_L' drops to around 12 (which is consistent to the simulation results in Fig. 5.6 and Fig. 5.7), Q_{tank1}' and Q_{tank2}' are calculated to be around 4.1 and 3.9, and 4.3 and 3.5 in the low-k and high-k states, respectively. From Eqs. (5.9a) and (5.9b), it can be seen that Q_{tank1}' is always larger than Q_{tank2}', and the difference between Q_{tank1}' and Q_{tank2}' can be reduced by increasing ω_2'/ω_1' or decreasing k_{12}' when k is small. As such, the proposed allocation of the frequency bands in the MT-VCO also helps reduce the difference between Q_{tank1}' and Q_{tank2}' by enlarging the ω_2'/ω_1' ratio.

5.3.3 Phase Noise

The noise-shaping property of a transformer-based LC tank is basically the same as that of a second-order LC tank within a narrow bandwidth around the oscillation frequency. It follows that the phase noise of the proposed MT-VCO in either the low band or the high band can also be obtained directly by using the time-variant phase-noise analysis result from [17]:

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T}{C'}\frac{\omega}{Q_{\text{tank1/2}}'\Delta\omega^2 A_{1/2}^2}(1+\gamma)\right] \tag{5.10}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, $C' = 0.5C_{1/2}'$ is the tank capacitance connected to either the primary coil or the secondary coil as shown in Fig. 5.1(a), $Q_{\text{tank1/2}}'$ is the tank Q from either the primary coil or the secondary coil, $\Delta\omega$ is the offset frequency from the oscillation frequency ω, γ is the MOS channel noise factor and $A_{1/2}$ is the output amplitude. From Eq. (5.10), it can be seen that the phase noise is directly related to the $Q_{\text{tank1/2}}'$. Compared with a conventional oscillator using a second-order LC tank with $Q_{\text{tank}} = 5$, the phase noise degradation of the proposed MT-VCO with $Q_{\text{tank1/2}}' = 4$ is only about 1 dB assuming that the maximum output voltage swing in the two oscillators are identical and that both oscillators are biased at the boundary of the voltage and current limited region to achieve the maximum output voltage swing.

5.3.4 Design Considerations and Design Procedure

From the analysis above, the design procedure of the MT-oscillator can be summarized as below:

1) Selecting and designing the geometrical dimensions of the primary and

the secondary coils for suitable values of L_1, L_2, and k_{12}. Since k_{12}' is dominant by k_{12} from Eqs. (5.4e) and (5.5e), for the same $\Delta k_{12}'$, larger k_{12} would results in larger frequency difference between the low-k and high-k states as can be seen from the plots in Fig. 5.2, which implies more effective coarse frequency tuning capability. However, for stability considerations, larger k_{12} requires larger ratio of ω_H' / ω_L'. This would cause a larger frequency gap between the low frequency band and the high frequency band of the low-k state, which however cannot be covered effectively even by employing the low band of the low-L state. As a result, the frequency tuning range can be discontinuous**.**

2) After fixing the design parameters of L_1 and L_2, the spaces between L_1 and L_A and L_B and between L_2 and L_A and L_C can be designed to guarantee that $k_{1A} = k_{1B}$ and $k_{2A} = k_{2C}$. As discussed earlier, the choices of the absolute values of k_{1A} or k_{2A} are the trade-off between the coarse frequency tuning capability and the Q_{L1}' and Q_{L2}'.

3) Designing the ratios between the switch sizes of M_A, M_B, and M_C to make sure that $C_{off,A}$, $C_{off,B}$, $C_{off,C}$ are properly chosen to guarantee that $\omega_A = \omega_B = \omega_C$. The choice of the absolute value of the switch sizes is to obtain high Q_{L1}' and Q_{L2}' while still preventing Q_{L1}' and Q_{L2}' from dropping at the desired maximum oscillation frequency.

Fig. 5.10 shows the layout of the switched-triple-shielded transformer with all the five coils being implemented by the top thick metal. The W/L ratios of M_A, M_B and M_C are designed to be 27.5μm/0.06μm, 17.5μm/0.06μm, 42.5μm/0.06μm, respectively, all with 2.5-μm finger widths. Odd finger numbers are used to keep the same parasitic capacitance at the drain and the source. The source and drain of the switches M_A, M_B

and M_C are biased to the opposite logic levels of the gate voltages through the center taps of the shielding inductors to reduce the parasitic junction capacitance when the switches are off. By doing so, the biasing resistors connected to the drain and source in the conventional designs can be eliminated, which helps prevent further degradation of Q_{L1}' and Q_{L2}'.

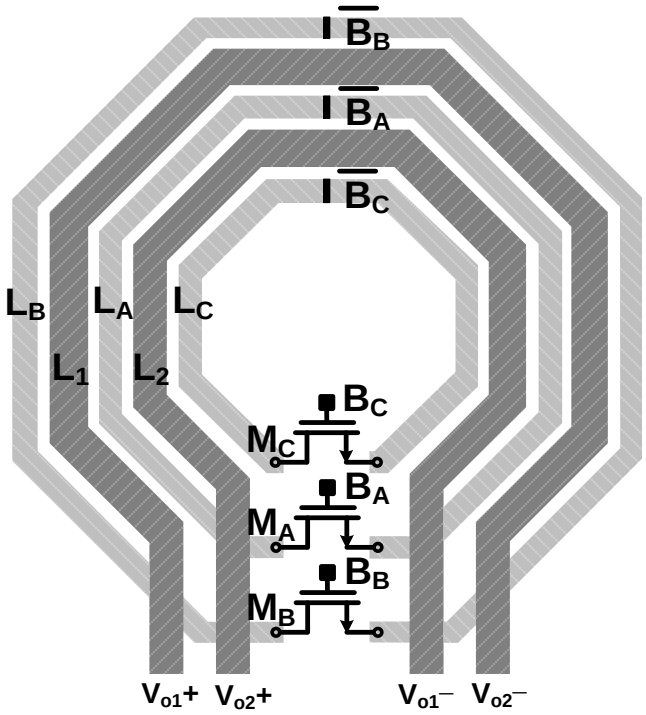


Fig. 5.10 Layout of the proposed switched-triple-shielded transformer

Fig. 5.11 shows the electromagnetic simulation results of the effective inductances and Q's for the primary and secondary coils of the triple-shielded transformer. L_1' and L_2' are 105 pH and 75 pH in both the low-k and high-k states and 80 pH and 50pH in the low-L state, respectively. k_{12}' is reduced from 0.35 to 0.15 from the high-k to the low-k state. Q'_{L1} and Q'_{L2} are around 10 and 12 in all the three states, which are still much higher than the varactors' Q at the target mm-Wave frequencies.

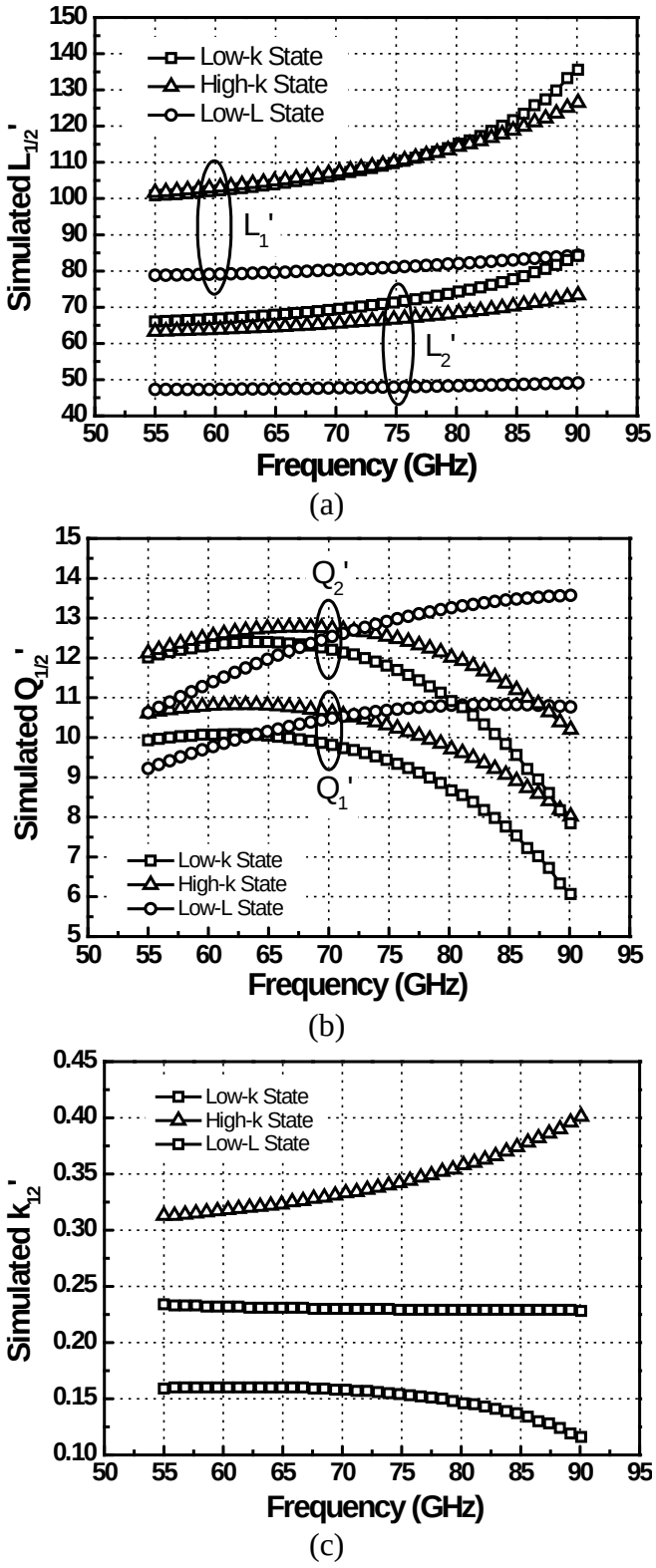


Fig. 5.11 Electromagnetic simulation results of the proposed triple-shielded transformer: (a) inductances, (b) quality factor Q's, (c) magnetic coupling coefficients

5.4 Experimental Results

The proposed MT-VCO is fabricated in a 1P6M LP 65nm CMOS process and draws 7 to 9 mA from 1.2 V supply. The DC gate bias voltages for M_A, M_B, and M_C are the same as the supply voltage. Fig. 5.12 shows the chip micrograph occupying a core area of 0.25×0.12 mm^2.

Table 5.1 summarizes the control logics of the switches in the shielding coils and the biasing currents for the negative-g_m cell connecting to the primary and the secondary coils of the transformer tank for 6 different modes associated with the 3 different states. The final implementation uses $B_BB_AB_C$ = 011 in Mode 2 and $B_BB_AB_C$ = 001 in Mode 5 instead of $B_BB_AB_C$ = 010 and $B_BB_AB_C$ =101 to obtain large ω_2 / ω_1 ratios to shift up the frequency tuning range in Mode 2 and minimize the tanks' Qs degradation in Mode 5 as discussed in Section 5.3, respectively.

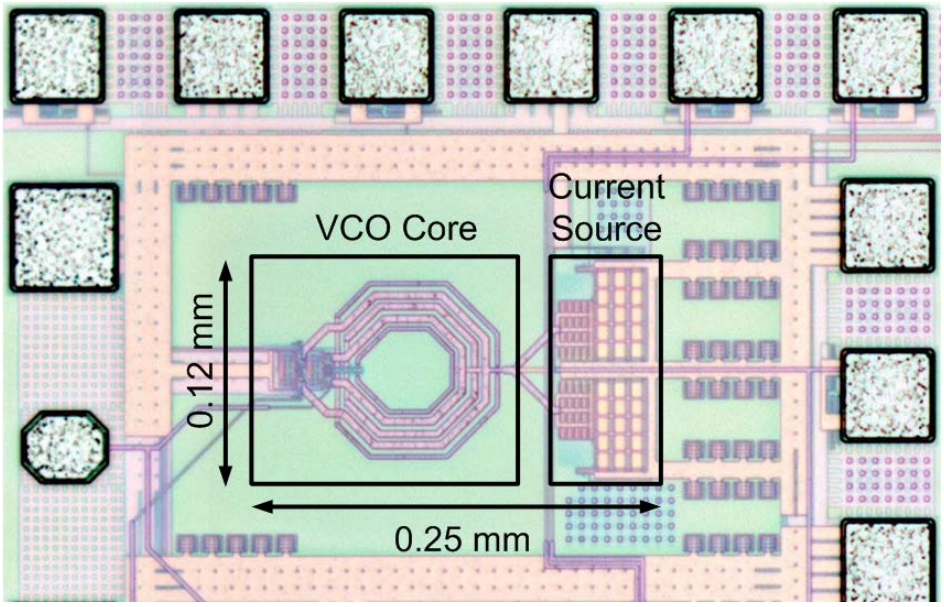


Fig. 5.12 Chip micrograph of the proposed MT-VCO

Table 5.1 Control logics and arrangement for mode selection

	Mode 1	Mode2	Mode 3	Mode 4	Mode 5	Mode 6
$B_BB_AB_C$	101	011	111	010	001	111
I_1	On	On	On	Off	Off	Off
I_2	Off	Off	Off	On	On	On
States	High-k	Low-k	Low-L	Low-k	High-k	Low-L
Bands	Low Band			High Band		

Fig. 5.13 shows the measured frequency tuning range as functions of the varactor's tuning voltage for the different modes. As shown in both Eqs. (5.1a) and Fig. 5.2(a), ω_L is not so sensitive to the change of k_{12} when k_{12} is small compared with ω_H. As such, the operating frequency in Mode 1 and 2 are almost the same as expected. Fig. 5.14 shows the measured phase noise over the entire frequency tuning range. Fig. 5.15 shows the phase noise plots after down-converting the VCO output by V-band and W-band balanced mixers. Finally, Table 5.2 summarizes and compares the measured performance of the presented MT-VCO with that of the recently reported state-of-art mm-Wave CMOS VCOs. The figure-of-merit (FOM) and figure-of-merit with tuning range (FOM_T) are defined as:

$$\mathrm{FOM} = \mathrm{PN} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{\mathrm{P_{diss}}}{1\mathrm{mW}}\right) \tag{5.11}$$

$$\mathrm{FOM_T} = \mathrm{PN} - 20\log\left(\frac{f_0}{\Delta f}\cdot\frac{\mathrm{TR}[\%]}{10}\right) + 10\log\left(\frac{\mathrm{P_{diss}}}{1\mathrm{mW}}\right) \tag{5.12}$$

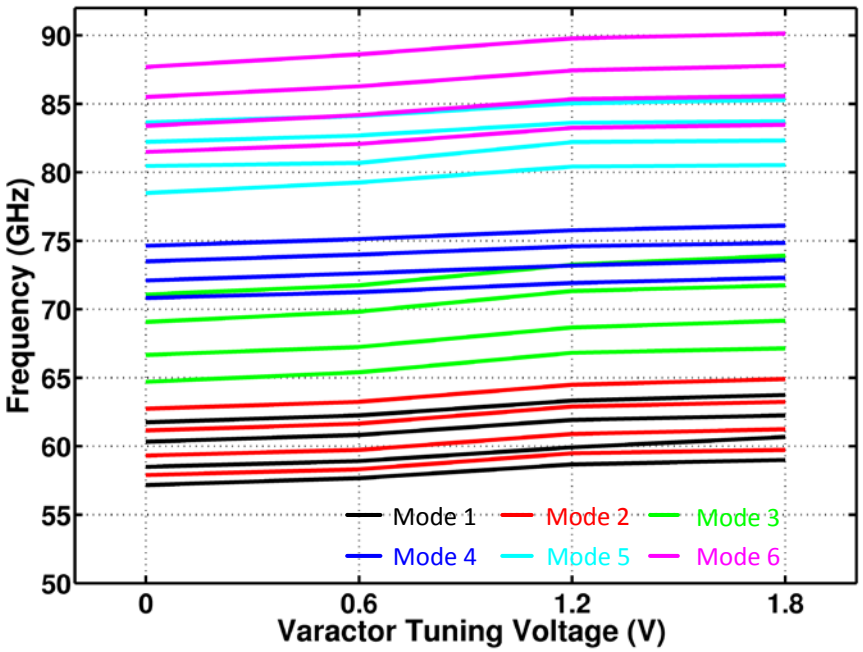


Fig. 5.13 Measured frequency tuning range

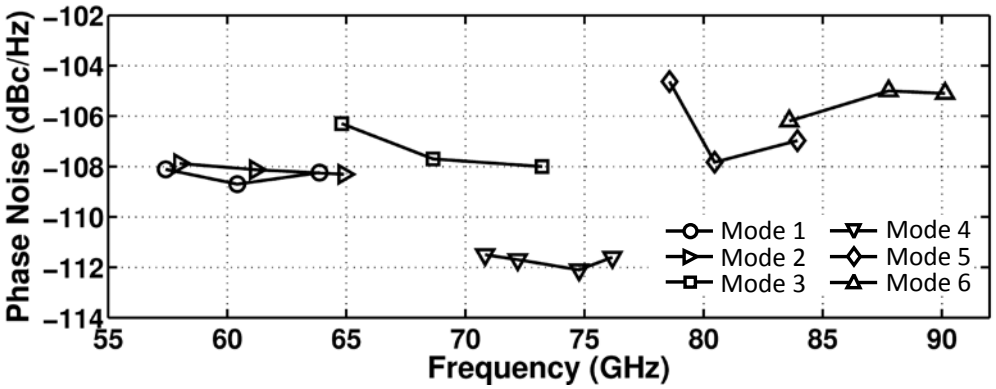


Fig. 5.14 Measured VCO phase noise at 10MHz offset frequency

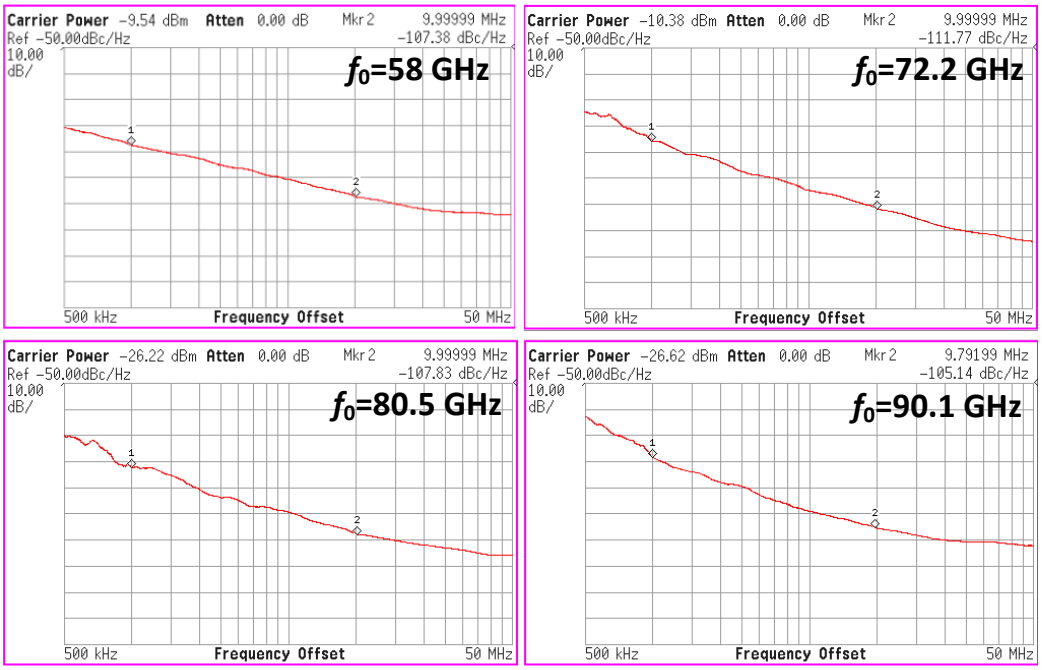


Fig. 5.15 Measured VCO phase noise as functions of offset frequency at different carrier frequencies

5.5 Conclusion

In this chapter, a switched-triple-shielded transformer is proposed to effectively change the magnetic coupling coefficient in a transformer-based dual-band VCO to increase the frequency tuning range. Based on the proposed switched-triple-shielded transformer, a magnetically-tuned multi-mode mm-Wave VCO with ultra-wide frequency tuning range is successfully demonstrated in 65 nm CMOS process. Drawing 7 mA to 9 mA at 1.2 V supply, the presented multi-mode VCO achieves a continuous ultra-wide frequency tuning range of 44.2% from 57.5 to 90.1 GHz while still occupying small chip area with a single multiple-port transformer. The measured phase noise across the entire frequency range is between -104.6 to -112.2 dBc/Hz @10 MHz frequency offset, corresponding to FOM_T between -184.2 and -192.2 dBc/Hz.

Table 5.2 Performance summary and comparison of the MT-VCO

Ref.	Tech.	Center Freq. (GHz)	TR	Power (mW)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Area (mm^2)
[1]	65nm SOI	70.2	9.6%	5.4	-106.1 @10MHz	-175.8	-175.4	0.0027
[2]	90nm CMOS	58.4	9.6%	8.1	-91@1MHz	-177.2	-176.6	0.0077
		61.7	4.9%	1.2	-90@1MHz	-185	-178.6	
[3]	65nm CMOS	58.2	7.6%	22(1)	-95/-97 @1MHz	-177/ -179	-174.5/ -176.5	0.075
[4]	0.13μm CMOS	59	9.8%	9.8	-89@1MHz	-174.5	-174.4	0.24(3)
		98.5	2.5%	7-15	-102.7@10MHz	-174.1	-162.2	
		105.2	0.2%	7.2	-97.5@10MHz	-169.4	-135.0	
[5]	0.13μm CMOS	60	16.7%	30	-97.1@1MHz	-177.9	-182.3	0.172(4)
[6]	65nm CMOS	67.1	27%	5.8	-89.5@1MHz	-178.4	-187	0.031
[7]	90nm CMOS	48	16.7%	22.7(1)	-85@1MHz	-165.1	-169.5	N/A
[8]	90nm CMOS	61.05	9.27%	10.6	-90.1@1MHz	-174.4	-174.9	0.01
[9]	0.13μm CMOS	50.3	6.8%	35(2)	-127.8@10MHz	-186.4	-183.0	0.18(3)
		58.5	9%	34(1)	-120.6@10MHz	-180.6	-179.7	0.1(3)
This Work	65nm CMOS	73.8	44.2%	8.4 -10.8	-104.6/-112.2 @10M	-172/ -180	-184.2/ -192.2	0.03

(1) 4-phase output (2) 8-phase output (3) Area including pads (4) Area including the divider

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Chapter 6

Wide-Band Millimeter-Wave Frequency Divider

6.1 Introduction

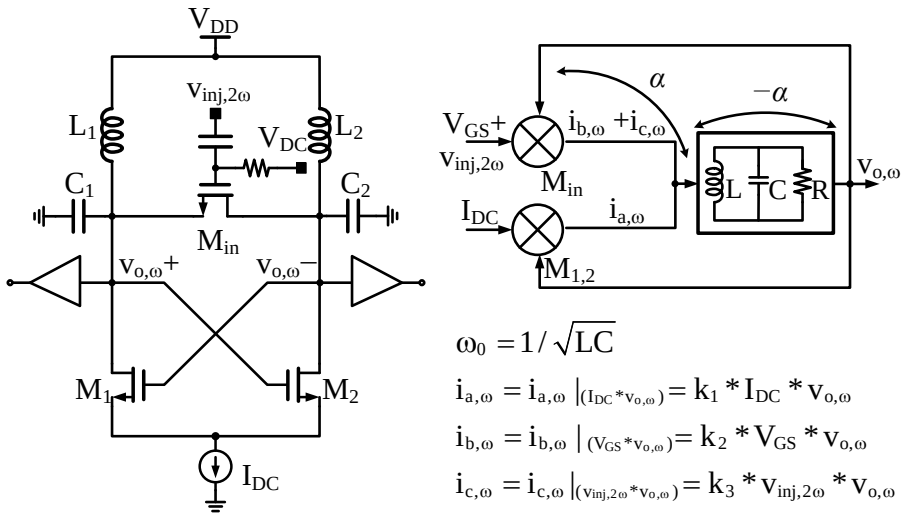
Frequency dividers are key components in frequency synthesizers for mm-wave applications. Compared with Miller frequency dividers and CML static dividers, injection-locked frequency dividers (ILFDs) usually feature high operation frequencies at low power consumption, but their locking range is very limited. Recently, although many design techniques have been reported to increase the locking range of ILFDs [1]-[5], their locking ranges are still insufficient to cover the required tuning range for the millimeter Wave (mm-Wave) applications from 57 GHz to 66 GHz with enough margins for PVT variations.

In this chapter, a transformer-based self-frequency-tracking (SFT) technique is proposed to tackle the problem while still consuming low power.

6.2 Locking Range Limitation of the Conventional Injection-Locked Frequency Divider (ILFD)

The schematic and the behavioral model of a conventional ILFD based on a simple LC tank are shown in Fig. 6.1(a) and (b). The transistors M_{in} and $M_{1,2}$ act as single-balanced mixers, and the total current injected into the tank contains three components:

$i_{a,\omega}|_{(I_{DC}*v_{o,\omega})}$, $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$, and $i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}$, which are the mixing products of the output voltage $v_{o,\omega}$ with the DC bias current I_{DC}, with the DC gate-to-source bias V_{GS} of M_{in}, and with the ac input voltage $v_{inj,2\omega}$, respectively. Since I_{DC} and V_{GS} are mixed with the signals at two differential nodes $v_{o,\omega}+$ and $v_{o,\omega}-$, their mixing products tend to cancel each other. At the locking frequency, the total currents $i_{o,\omega} = i_{a,\omega}|_{(I_{DC}*v_{o,\omega})} + i_{b,\omega}|_{(V_{GS}*v_{o,\omega})} + i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}$ injected into the LC tank should be capable of creating enough phase shift α to compensate the phase shift $-\alpha$ by the LC tank to meet the phase condition. Besides, the cross-coupled pair M_1 and M_2 needs to provide enough gain to compensate the losses from the tank and from M_{in} so as to meet the gain condition. The current component $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ impairs the gain condition since it is in the opposite direction to $i_{a,\omega}|_{(I_{DC}*v_{o,\omega})}$.



(a) (b)

Fig. 6.1 Conventional ILFD: (a) schematic, and (b) the behavioral model

As shown in the phasor diagrams in Fig. 6.2(a), when the effective g_m of M_{in} is small, corresponding to a small size $(W/L)_{M_{in}}$ or a small gate bias V_{GS} of M_{in}, the

conventional ILFD works in the phase-condition-limited (PCL) region. The maximum locking range is decided by the maximum phase shift α_{max} that can be provided by $i_{o,\omega}$. So the locking range can be enhanced by either increasing $|i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}|$ or $|i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}|$. Since $i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}$ and $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ are the outputs of the same mixing transistor M_{in}, they both increase with the increasing of $(W/L)_{M_{in}}$ or V_{GS} if M_{in} stays in the saturation region. When $(W/L)_{M_{in}}$ or V_{GS} becomes large enough, the divider enters into the gain-condition-limited (GCL) region, and the locking range can not be further increased without increasing current consumption even if the $i_{o,\omega}$ can create enough phase shift. Moreover, large V_{GS} would eventually push M_{in} into the triode region, which would degrade the effective g_m and thus $|i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}|$. Consequently, an optimal V_{GS} exists for the maximum locking range for fixed $(W/L)_{M_{in}}$ and current consumption.

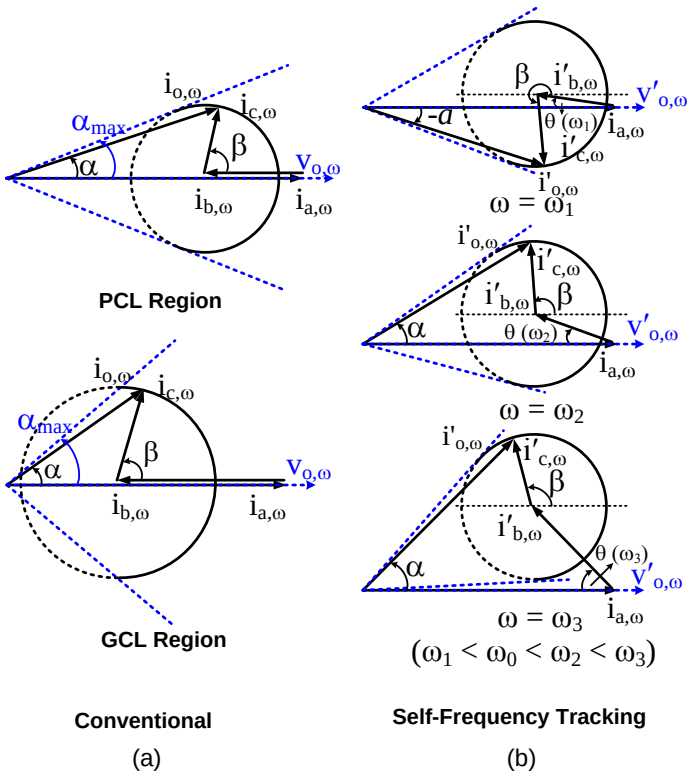


Fig. 6.2 Phasor diagrams of (a) the conventional ILFD and (b) the SFT-ILFD

6.3 Proposed Self-Frequency-Tracking ILFD

Fig. 6.3(a) and (b) show the schematic and the behavioral model of the presented SFT-ILFD based on a transformer tank. The currents are injected through the secondary coil (L_2 and L_4) while the negative g_m cell is connected to the primary coil (L_1 and L_3).

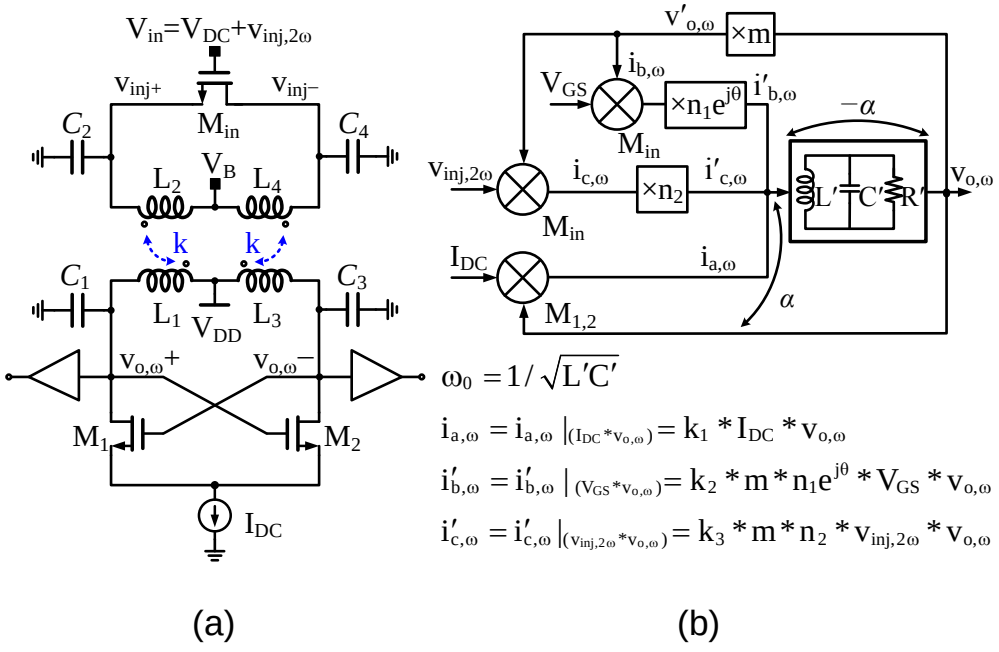


Fig. 6.3 The proposed SFT-ILFD: (a) schematic, and (b) the behavioral model

As shown in the phasor diagram in Fig. 6.2(b), where L', C' and R' represent the effective tank inductance, capacitance, and loss, respectively, seen from the primary coil, the transformer tank changes the amplitude of $v_{o,\omega}$ and $i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}$ by factors of $m = k\sqrt{L_2/L_1}$ and n_2. For the injected current $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$, both the amplitude and the phase are changed by multiplying it with $n_1 e^{j\theta}$, which creates a phase shift θ between $i'_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ and $-i_{a,\omega}|_{(I_{DC}*v_{o,\omega})}$. Compared with the conventional ILFD where there is no phase shift between $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ and $-i_{a,\omega}|_{(I_{DC}*v_{o,\omega})}$, the existence of θ helps relax both the phase and gain conditions and thus increase the locking range without the needs to

increase $|i'_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}|$ when $\omega>\omega_0$ ($\omega_0 = 1/\sqrt{L'C'}$).

The phase shift θ can be derived by using the equivalent circuit shown in Fig. 6.4(a). The injected currents $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ and $i_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}$ from M_{in} are represented by the transconductance Y_1 and $Y_2e^{j\beta}$, respectively. When converted from the secondary coil L_2 to the primary coil L_1, the transconductance representations of the equivalent currents $i'_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ and $i'_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}$ changes to Y_1' and $Y_2'e^{j\beta'}$, and C_2 changes to C_2'. The Y_1', Y_2' and C_2' can be expressed as below:

$$Y_1' = n_2 \cdot \{Y_1 + j[a(1-a)\omega C_2 - a(1+a)(Y_1^2 - Y_2^2)/(\omega C_2)]\} \tag{6.1}$$

$$Y_2' = n_2 Y_2 \tag{6.2}$$

$$C_2' = k^2 \frac{L_2}{L_1} C_2 \tag{6.3}$$

where ω is the output frequency, C_2 is the total parasitic capacitors at the drain or source of M_{in}, $n_2 = k^2 \cdot \frac{L_2}{L_1} \cdot \frac{1}{(a/\omega C_2)^2 (Y_1^2 - Y_2^2) + (1-a)^2}$, $a = \omega^2 L_2 C_2 (1-k^2)$ and k is the coupling coefficient between L_1 and L_2. From (6.1), a phase shift $\theta = \arctan\{[a(1+a)(Y_1^2 - Y_2^2)/(\omega C_2) - a(1-a)\omega C_2]/Y_1\}$ has been created between $i'_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ and $i_{b,\omega}|_{(V_{GS}*v_{o,\omega})}$ or $-i_a|_{(I_{DC}*v_{o,\omega})}$ after passing through the transformer tank. Fig. 6.4(b) plots the θ as a function of frequency for different C_2 values. It is important to note that θ increases with frequency. From the phasor diagrams shown in Fig. 6.2(b), this self-frequency-tracking property of θ helps increase the locking range further because it increases the maximum phase shift α_{max} provided by $i_{o,\omega}$ even with $|i'_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}|$ being constant when input frequency increases.

Usually, it is difficult to increase $|i'_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}|$ to boost the maximum operating

frequency because both the input voltage swing and conversion gain of the mixing transistor M_{in} are significantly degraded at high frequencies. On the other hand, by exploiting the frequency-dependent phase shift θ, the proposed self-frequency tracking technique can boost the maximum operating frequency without the need of increasing $|i'_{c,\omega}|_{(v_{inj,2\omega}*v_{o,\omega})}|$. As shown in Fig. 4(b), increasing C_2 also helps increase θ at the highest frequency end but at the expense of a lower operating frequency. In this design, C_2 is parasitic capacitance of around 20fF. When $\omega<\omega_0$, although θ would impair the locking range, the degradation is limited by a smaller θ due to the frequency-dependent property. As a result, the total locking range is still enhanced.

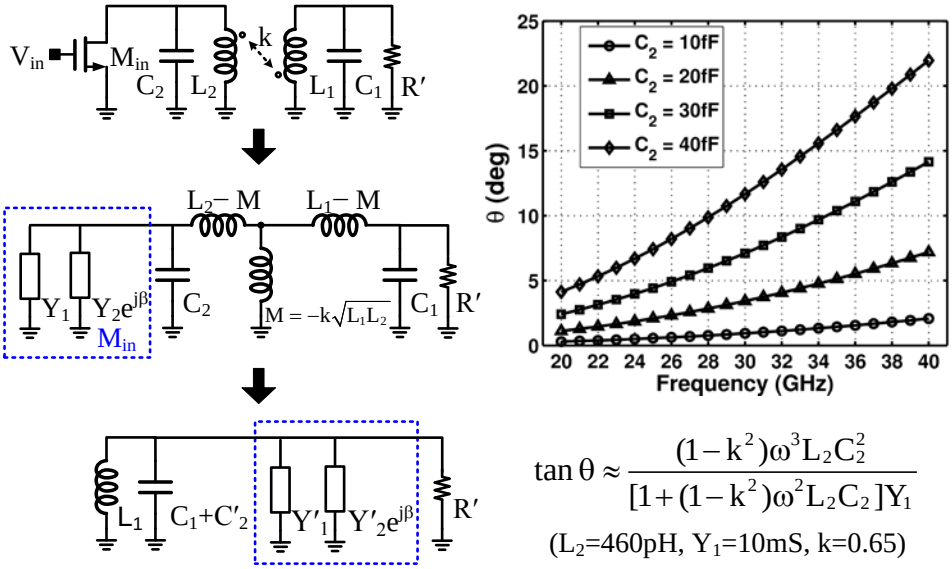


Fig. 6.4 (a) The equivalent circuits of transformer tank to derive the phase shift θ. (b) The plots of θ as functions of frequency for different C_2 values.

Moreover, in the conventional ILFD, an AC coupling capacitor is needed between VCO's output and ILFD's input nodes to obtain optimal $V_{GS}=V_{DC}-V_{DD}$ bias condition of M_{in} since the source and drain voltage of M_{in} is fixed to V_{DD}. At mm-Wave

frequencies, the use of AC coupling capacitor adds parasitic capacitance and degrades the input signal swing, which in turn limits the locking range. In the presented SFT-ILFD, since the currents are injected through the secondary coil instead of directly into the output nodes as in the conventional ILFD, the source and drain of M_{in} can be biased independently ($V_{GS}=V_{DC}-V_B$), which eliminates the AC coupling capacitor needed in the conventional ILFD.

6.4 Experimental Results

To verify the effectiveness of the proposed SFT technique, a SFT-ILFD is fabricated in a 65nm 1P6M LP CMOS process. The chip micrograph is shown in Fig. 6.5. The core area of the SFT-ILFD is 0.22×0.11 mm^2. The size of input transistor M_{in} is 13μm/0.06μm with 1 μm finger width. The odd finger number is used to keep the parasitic capacitance of the drain and the source symmetrical. The transformer parameters from electromagnetic simulation are $L_1 = L_3$= 340 pH, $L_2 = L_4$= 460 pH with $Q_1 = Q_3$= 17, $Q_2 = Q_4$= 10, and k = 0.65 at 30 GHz.

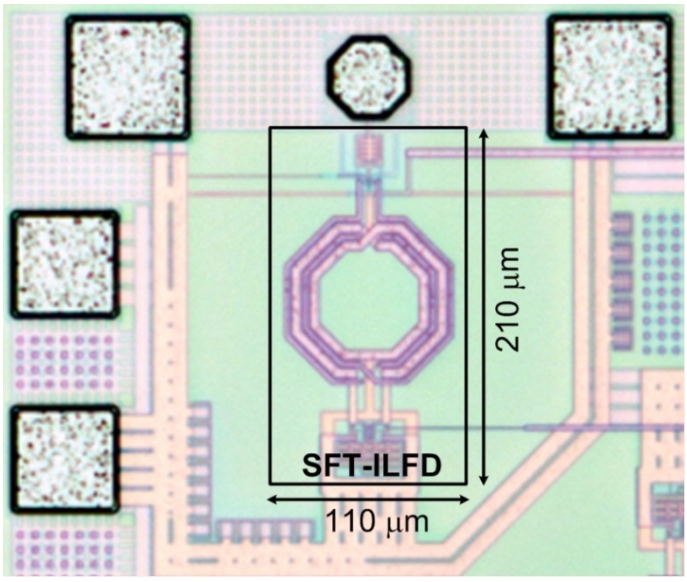


Fig. 6.5 Chip micrograph of the proposed SFT-ILFD

Fig. 6.6 shows the measured input sensitivity curve. Since the maximum output frequency provided by the signal generator is only 67 GHz, so within the input frequency range lower than 67GHz, the signal generator is directly connected to the SFT-ILFD to generate the input signal, while a frequency doubler and is used to generate the input frequency higher than 67 GHz. The attenuator after the frequency doubler is employed to adjust the input power since the output power from the frequency doubler is fixed. Consuming 1.9 mW from a 0.8 V supply, the input locking range with 0 dBm input power is measured to be 29% from 53.7 to 72.0 GHz with V_{GS} = 0.75 V.

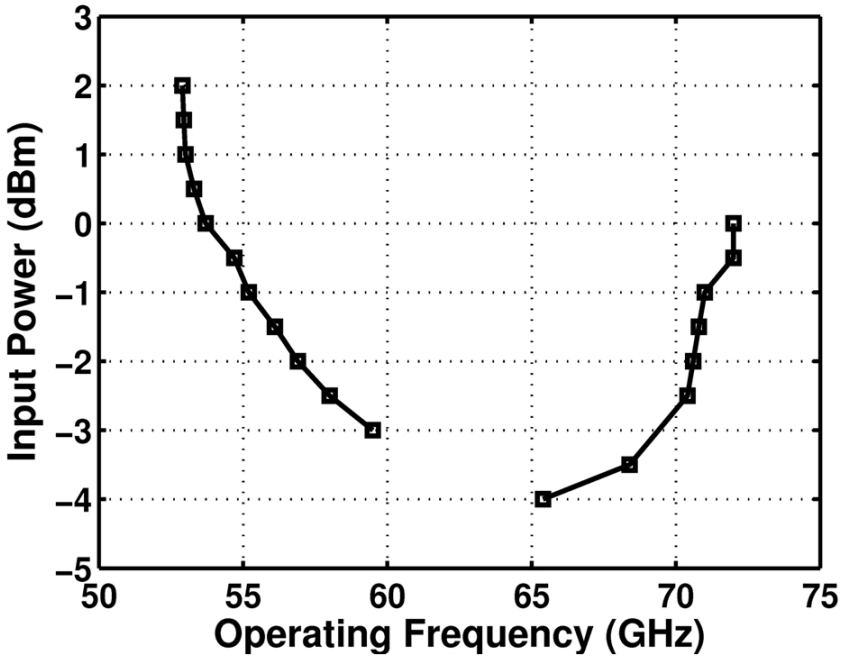


Fig. 6.6 Measured input sensitivity curve of the SFT-ILFD

Fig. 6.7 shows the ILFD's output spectrum at the lowest and the highest input frequencies.

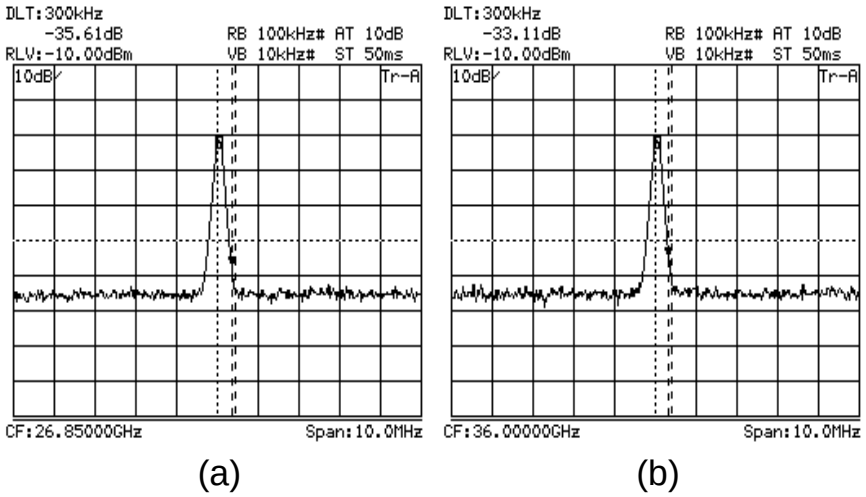


Fig. 6.7 Measured output spectrums at (a) the lowest (53.7 GHz) and (b) the highest (72.0 GHz) input frequency

Fig. 6.8 shows the measured locking range as a function of I_{DC}. It indicates that the locking range can be further increased at the cost of large power consumption.

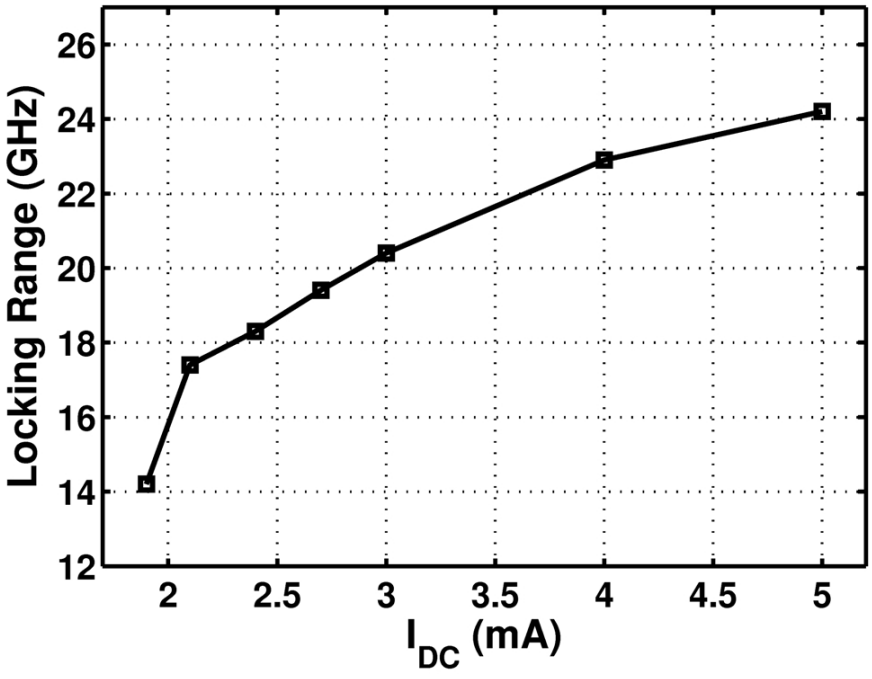


Fig. 6.8 Measured locking range as a function of I_{DC}. (V_{DD}=0.8V, V_{GS}=0.75V)

Table 6.1 summarizes and compares the measured performance of the SFT-ILFD to

that of the recently reported state-of-art wide-locking-range ILFDs. The figure-of-merit (FOM) are defined as:

$$\text{FOM} = \frac{\text{Locking Range (GHz)}}{\text{Power (mW)}} \tag{6.4}$$

6.5 Conclusion

In this chapter, a SFT transformer-based ILFD with enhanced frequency locking range is successfully demonstrated. By creating a frequency-dependent phase shift for the total current injected into the transformer tank, the SFT technique helps relax both the phase and gain conditions, thus increase the locking range of the ILFD. Implemented in 65nm CMOS, the presented frequency divider occupies a core area of 0.22×0.11 mm^2. When consuming 1.9 mW from 0.8 V supply, it achieves an input locking range of 29% from 53.7 to 72.0 GHz at 0 dBm input power and a corresponding FOM of 9.53, which to the best of our knowledge, is the highest reported to date among all the published CMOS frequency divider at 60 GHz.

Table 6.1 Performance summary and comparison of the SFT-ILFD

Ref.	ISSCC 09 [1]	ISSCC 09 [2]	CICC 10 [3]	JSSC 08 [4]	RFIC 11 [5]	This Work
Process	65 nm CMOS	0.13 μm CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS	65 nm CMOS
Supply Voltage (V)	1.1	0.8	1	N/A	1.2	0.8
Center Freq. (GHz)	132.6	63.3	55.5	57.1	58.8	62.8
Input Power (dBm)	-5	0	0	0	0	0
Input Frequency (GHz)	128.24 to 137	59.6 to 67	48.5 to 62.9	53.4 to 60.8	52.7 to 64.8	53.7 to 72
Locking Range (GHz)	8.76 (6.6%)	7.4 (11.7%)	14.4 (25.9%)	7.4 (13%)	12.1 (20.5%)	18.3 (29%)
Power (mW)	5.5	1.6	1.65	2.5**	8.6**	1.9
Core Area (mm^2)	0.05	0.0165	0.0157	0.015	0.0828	0.023
FOM*	1.6	4.63	8.73	3	1.4	9.53

* FOM=Locking range (GHz) / Power consumption (mW)

** Quadrature Outputs

*** W/ Pads

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Chapter 7

SDR All-Digital Frequency Synthesizer

7.1 System Architecture

Fig. 7.1 shows the architecture of the proposed SDR all-digital frequency synthesizer. The RF frequency synthesis part is based on the ADPLL proposed in Chapter 4 except for that the triple-band DCO is extended to a Q-DCO to generate the IQ signals. The 1.5 to 3 GHz output of the ADPLL is further divided down by two /2 dynamic dividers to generate IQ LOs from 0.375 GHz to 1.5 GHz.

For the mm-Wave frequency synthesis part, the 6 to 12 GHz IQ outputs for the Q-DCO is injected into a ×4 ILFM with wide frequency tuning range to generate the 24 to 48 GHz differential LOs. ILFM output is divided down by two /2 SFT-ILFDs to generate the 12 to 24 GHz IQ LOs. Here, even by using the locking range enhancement technique proposed in Chapter 6, a single SFT-ILFD can not cover the input range from 24 to 48 GHz with margin. So two SFT-ILFDs operating on different frequencies are used. The calibration loop is employed to align the free-oscillation frequency of the ILFM with 4 times of the injection frequency.

Both the analog PLL and the proposed ADPLL are implemented to generate IQ LOs from 375 MHz to 24 GHz and differential LOs from 24 to 48 GHz. The output frequency can be further divided down to generate IQ LOs below 375 MHz easily by using the dynamic divider if required. Another purpose of the analog PLL is to serve to measure the PTDC performance, since the measurement of the PTDC requires to

control the phase difference between the 8-phase inputs (CKV[7:0]) from DCO and the reference clock precisely.

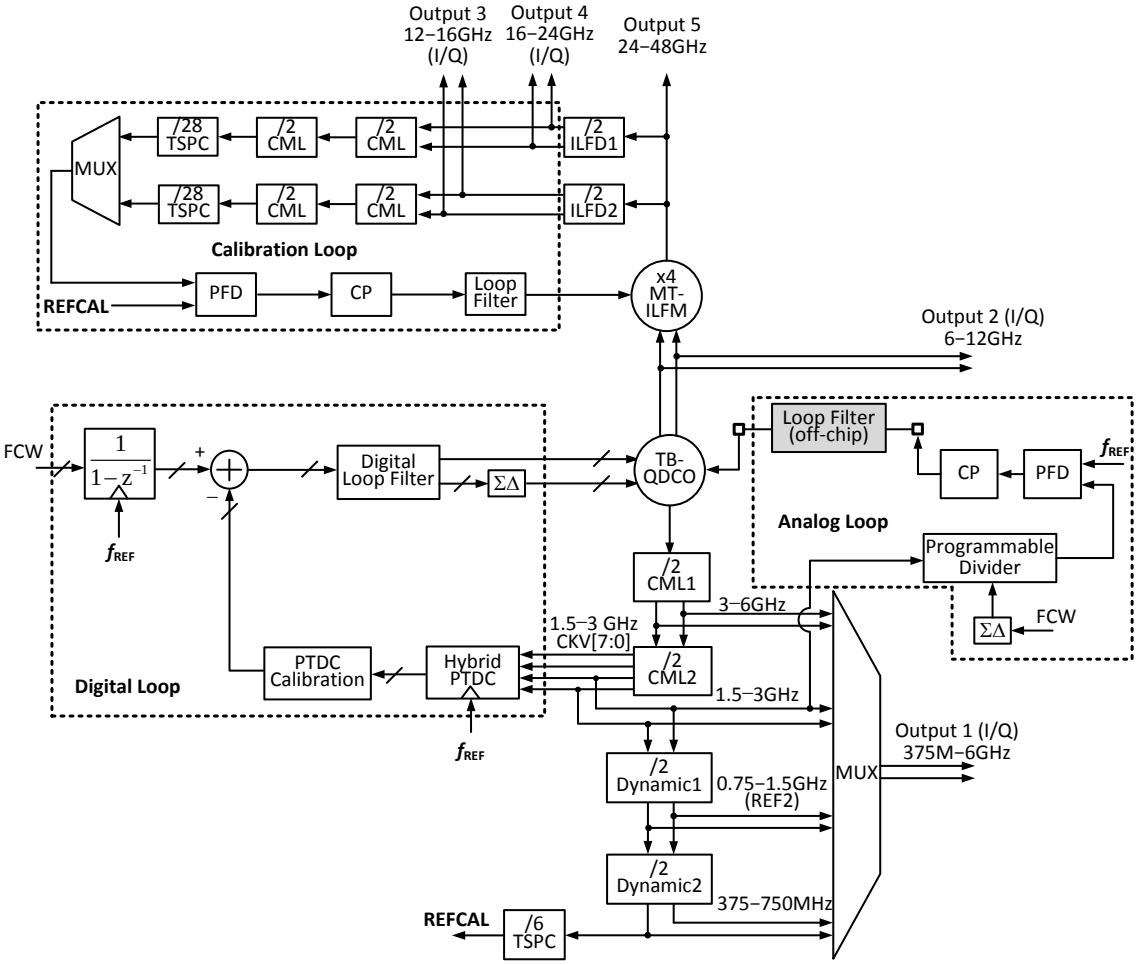


Fig. 7.1 System architecture of the proposed all-digital frequency synthesizer

7.2 Key Building Blocks

7.2.1 Quadrature DCO (Q-DCO)

Fig. 7.2 shows the schematic of the proposed Q-DCO. It is realized by coupling the DCO proposed in Chapter 4 in a ring structure through the NMOS transistor M_9 to M_{24}. The cascode transistor M_9, M_{10}, M_{13}, M_{14}, M_{17}, M_{18}, M_{21} and M_{22} are employed to create a phase shift in the loop to guarantee the outputs are always at the same IQ sequency.

Besides the active coupling, passive coupling by using capacitors between the output nodes of the VCO [1][2] or at the common-source nodes can also be used to couple the two oscillators to obtain IQ signals. The capacitive coupling avoids the use of noisy active devices, which will have better phase noise performance at the cost of larger capacitive loading at each tank, which will degrade the frequency tuning range. So to achieve a wideband tuning range here, the active coupling method is employed.

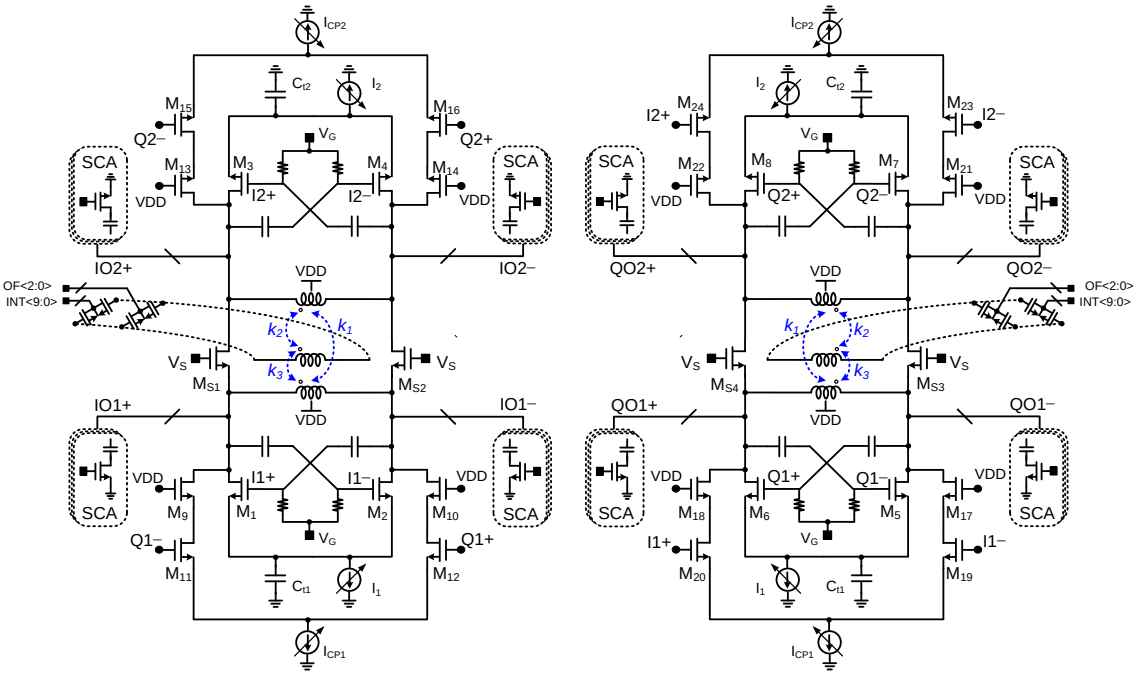


Fig. 7.2 Schematic of the proposed Q-DCO

7.2.2 ×4 Injection-Locked Frequency Multiplier (ILFM)

Fig. 7.3 shows the schematic of the ×4 ILFM. The switched-triple-shielded transformer is employed to achieve an ultra-wide frequency tuning range.

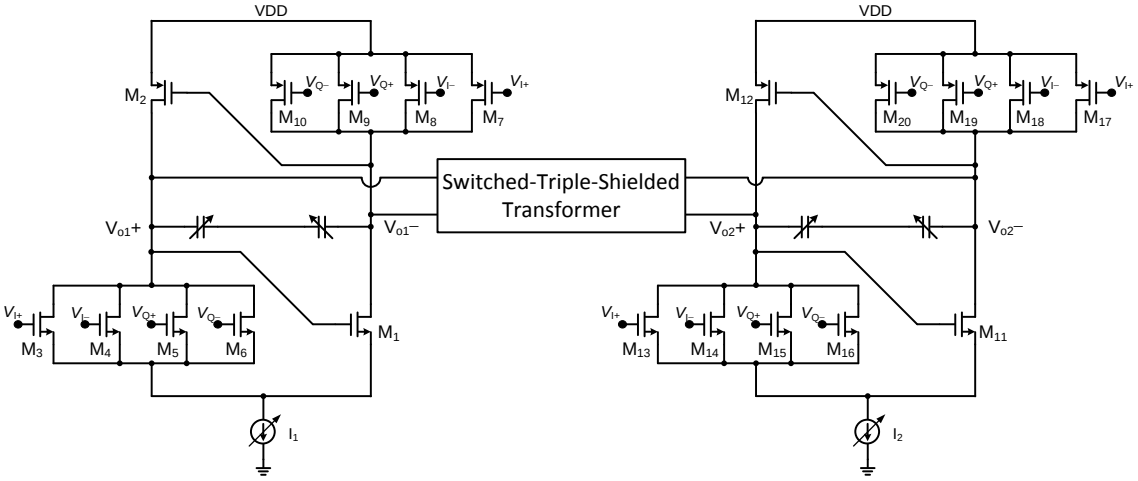


Fig. 7.3 Schematic of the ×4 ILFM with large frequency tuning range

The injection stage employs a four-push structure to generate the fourth harmonic of the input frequency. The use of both NMOS and PMOS injection stage help to reinforce the balance between the differential outputs, which would reduce the amplitude and phase unbalances [3].

7.3 Chip Implementation

The SDR all-digital frequency synthesizer is submitted for fabrication in the 1P9M 65-nm CMOS technology. Fig. 7.4 shows the chip micro-photo. The core area is 1.7 × 1.3 = 2.2 mm^2.

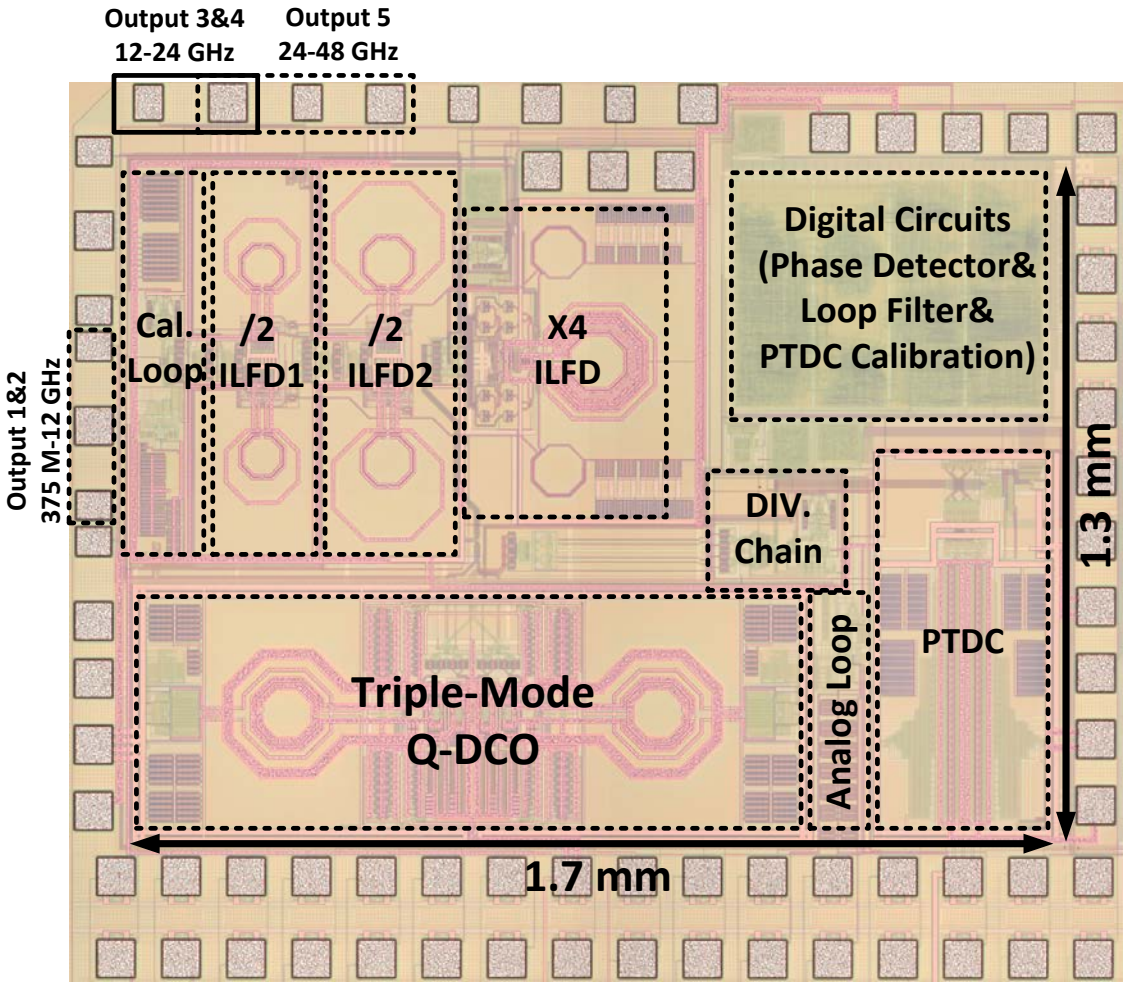


Fig. 7.4 Chip micrograph of the SDR all-digital frequency synthesizer

7.4 Experimental Results

7.4.1 Testing Setup

Fig. 7.5 shows the testing setup of the All-Digital SDR frequency synthesizer. Either the signal generator or the crystal oscillator can be used to provide the reference clock. The Lab Jack is used to generate the control signals for the shift register and the logic analyzer is employed to monitor the 10-bit outputs of the PTDC or the integer-bit of the digital loop filter. Parts of the analog filter composed by resistors and capacitors have been implemented off-chip on the PCB. Since the output PADs for RF frequency

generation (DC to 12 GHz) and Mm-Wave frequency generation (12 to 48 GHz) have been put at different side of the chip as shown in Fig. 7.4. Then they can be monitored by the probe 1 (40 GHz SGS probe) and probe 2 (60 GHz GSG probe) at the same time. The output spectrum and phase noise can be measured by the spectrum analyzer.

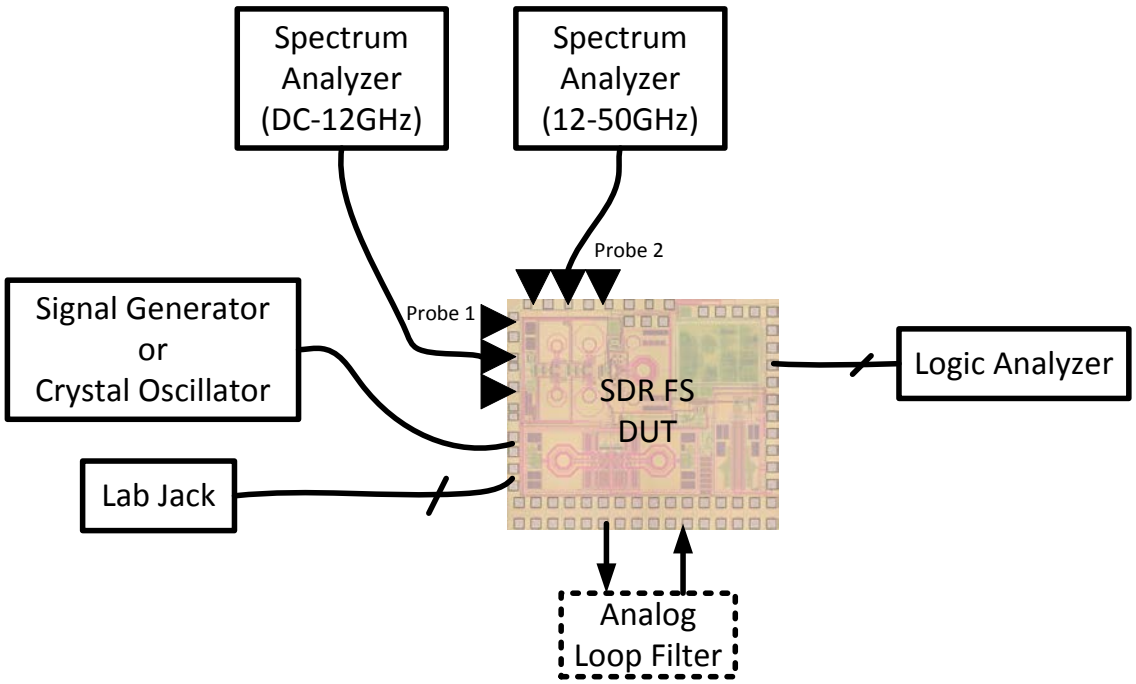


Fig. 7.5 Testing setup of the All-Digital SDR frequency synthesizer

7.4.2 Frequency Range

From the measurement, the Q-DCO generates the IQ signals from 4.9 to 12.9 GHz, which have enough margin to cover the design requirement which is from 6 to 12 GHz. After the divider chain cascaded by the CML and the dynamic dividers, the 306 MHz to 6.45 GHz IQ LO signals can be generated.

For the mm-Wave frequency synthesis, the x4 ILFM achieves frequency tuning range from 23 GHz to 46.5 GHz when freely runs. And the measurement shows the same locking range when injecting IQ signals generated by the Q-DCO from 5.75 GHz to 11.625 GHz into the x4 ILFM. The two /2 ILFMs together can cover the input

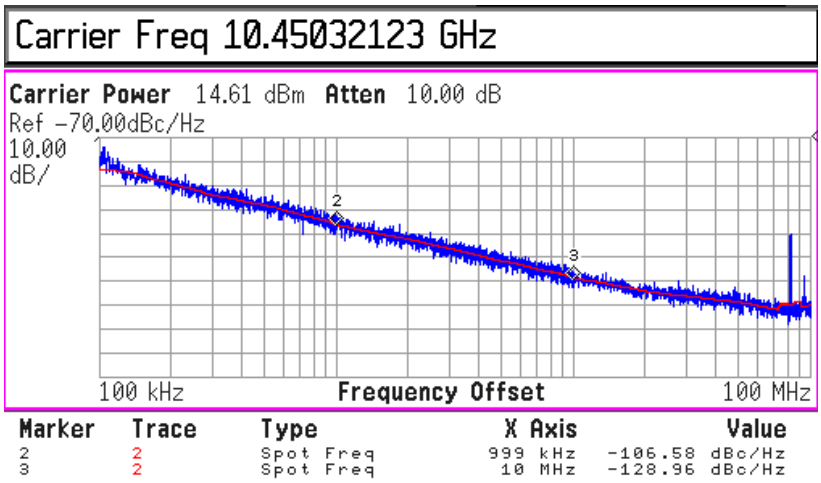
frequency range from 23 to 46.5 GHz, which generates the 11.5 to 23.25 GHz IQ outputs.

As a result, the proposed SDR frequency synthesizer can generate IQ LO signals from 306 MHz to 23.25 GHz and differential LO signals from 23.25 to 46.5 GHz. For low frequency end from 306 MHz down to DC, the dynamic divider with small power (<1 mA) and area (<300 μm^2) consumption can be easily duplicated. For the high frequency end, the drop of the highest operating frequency of the x4 ILFM from 48 to 46.5 GHz is due to the underestimation of the parasitic capacitance and mode inaccuracy of the switched transformer tank.

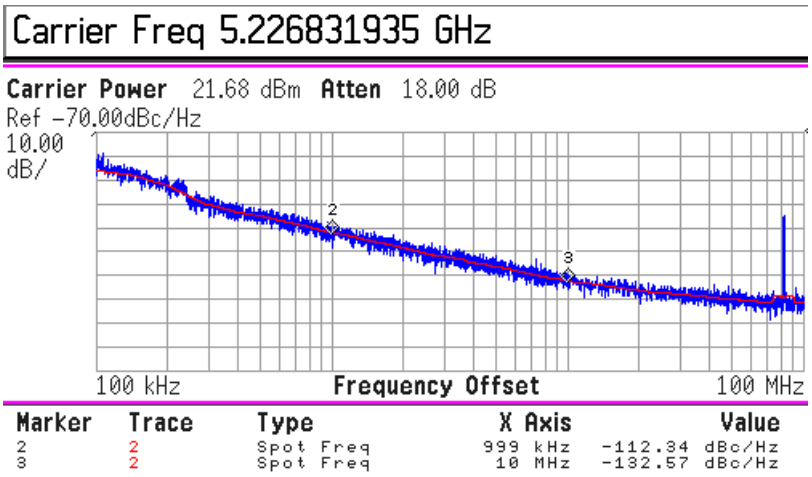
7.4.3 Open Loop Phase Noise

The open loop phase noise with free-running VCO and dividers was measured to verify the SDR out-band phase noise performance for different standards.

Fig. 7.6 (b) shows the measured open loop phase noise of the 5.225 GHz LO for 802.11a WLAN standard after divided-by-2 from the DCO output at 10.45 GHz. The phase noise at 1 MHz and 10 MHz offset are -112 and -132.5 dBc/Hz from 5.225 GHz carrier.



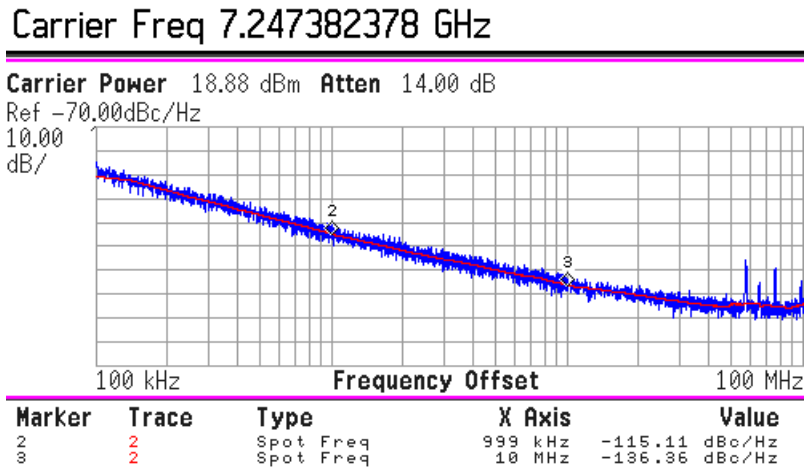
(a)



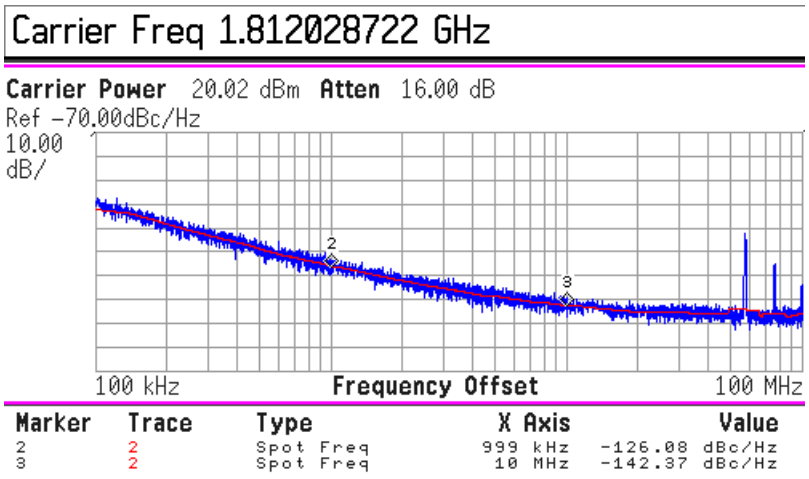
(b)

Fig. 7.6 Measured open loop phase noise for WLAN standard: (a) DCO output, (b) /2 CML divider output

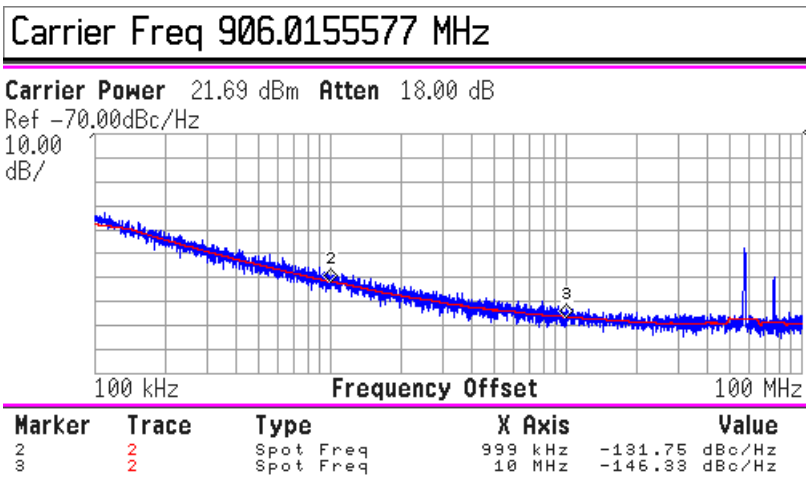
Fig. 7.7 shows the measured open loop phase noise of the 900 MHz and 1.8 GHz LO for cellular standards after divided-by-2 and divided-by-4 from the DCO output at 7.2 GHz. Respectively.



(a)



(b)



(c)

Fig. 7.7 Measured open loop phase noise for cellular standards: (a) DCO output, (b) /2 CML divider output, (c) /2 dynamic divider output

7.4.4 Close Loop Phase Noise

The close loop phase noise is measured with different loop bandwidth to trade-off the in-band and out-band phase noise to obtain the optimized integrated phase noise.

Fig. 7.8 shows the measure close loop phase noise at 12 GHz DCO output by using the analog PLL loop. The best in-band phase noise that can be achieved is -86.5 dBc/Hz at 100 kHz offset.

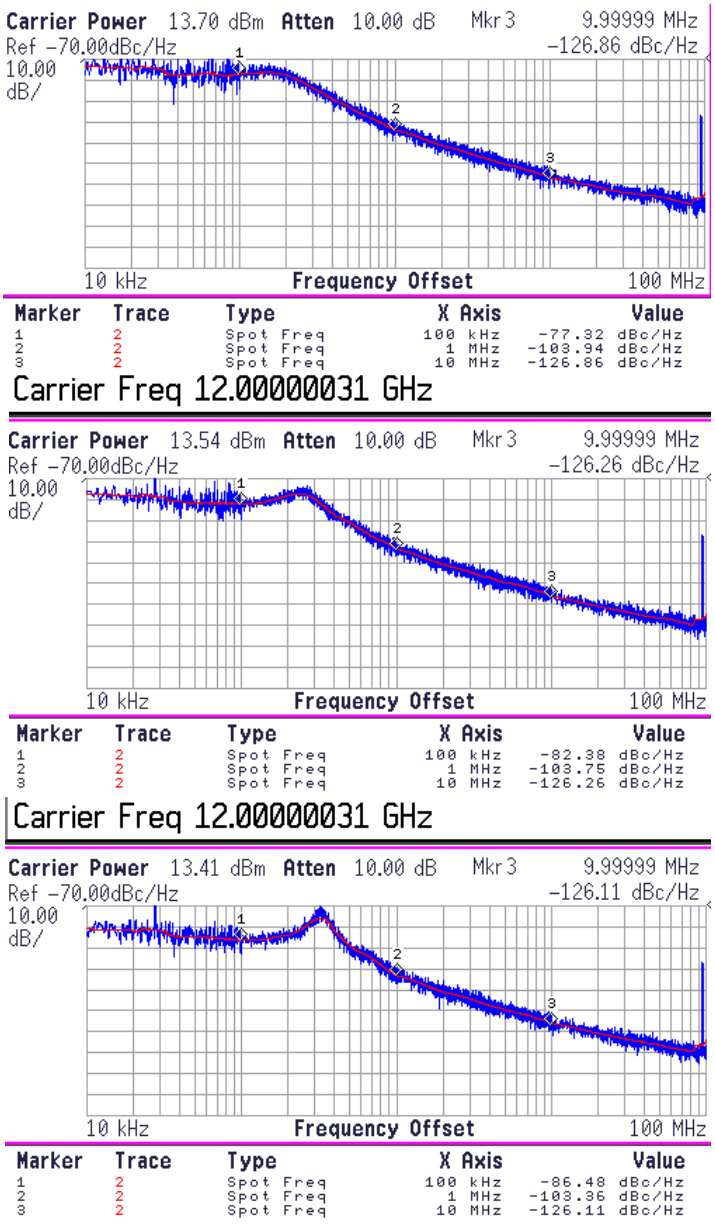


Fig. 7.8 Measured close loop phase noise at 12 GHz output

Fig. 7.9 shows the measure close loop phase noise for WLAN 802.11a at 5.4 GHz. The integrated phase noise from 50 kHz to 10 MHz is -35.2 dBc.

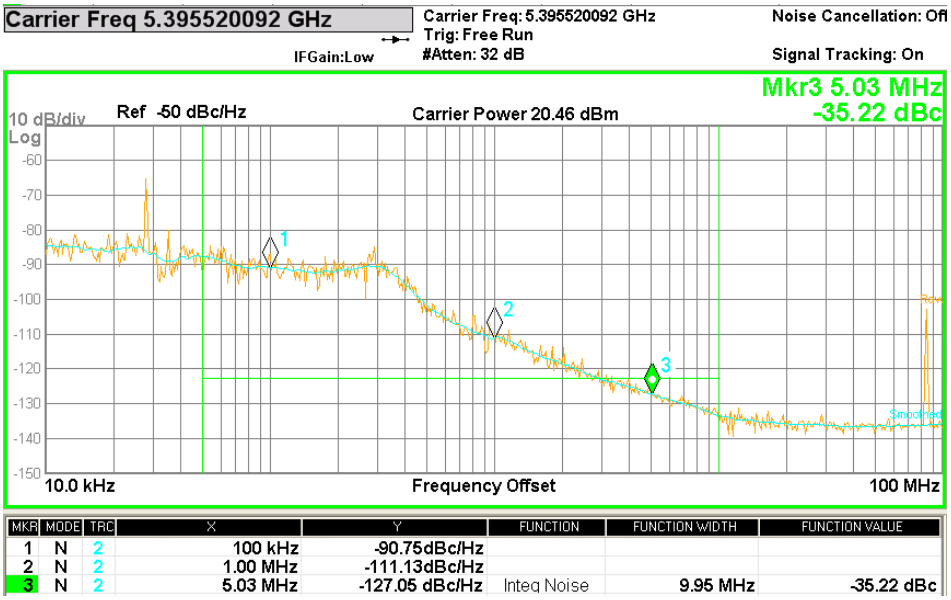


Fig. 7.9 Measured close loop phase noise for WLAN (802.11a) standard

Fig. 7. **10** shows the measured close loop phase noise for the 802.15.3c standard at 60 GHz by using the dual-conversion architecture. The integrated phase noise from 50 kHz to 10 MHz is -19 dBc.

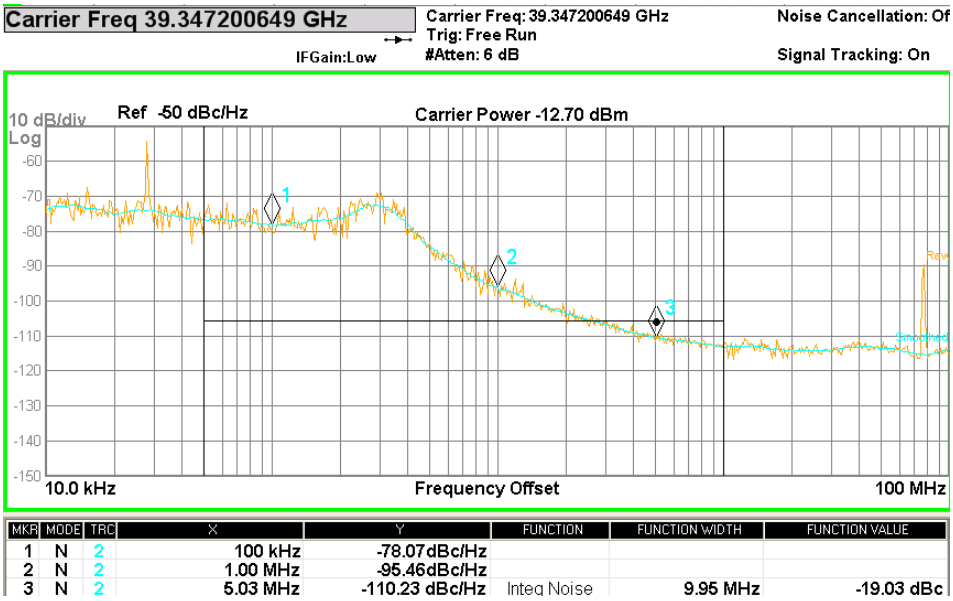
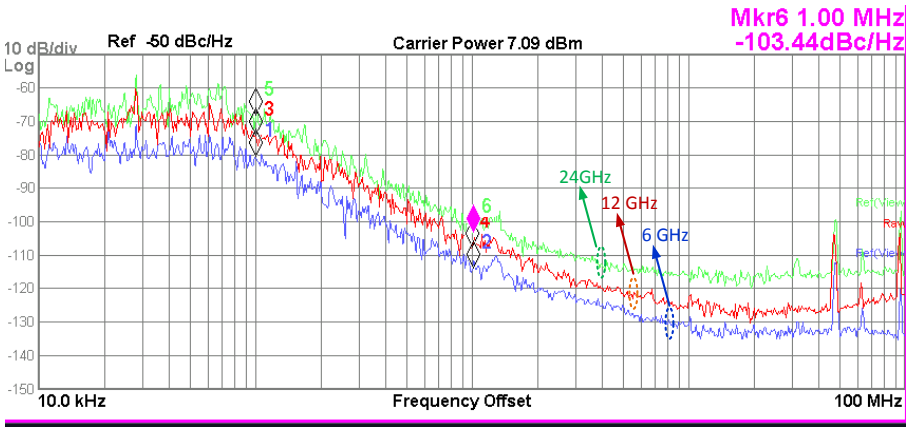


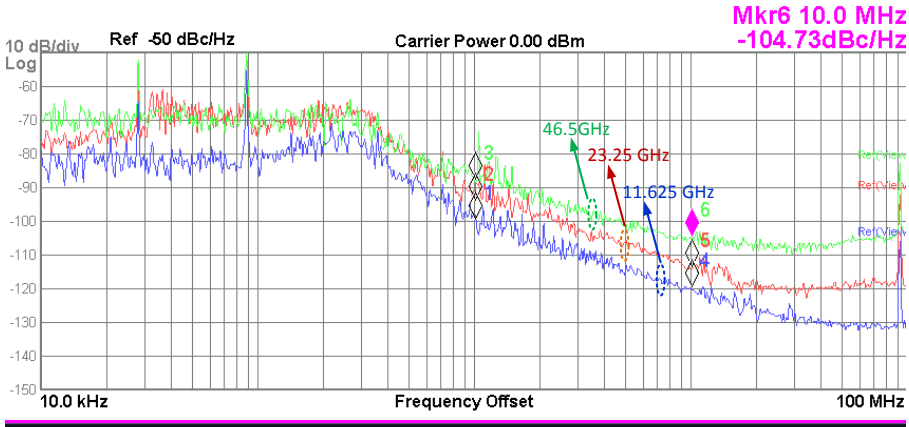
Fig. 7.10 Measured close loop phase noise for 802.15.3c standard

Fig. 7.11 and Fig. 7.12 shows the measured close loop phase noise at the x4 ILFM output and /2 ILFD2 output, respectively. The phase noise of the 6 GHz and 11.625 GHz injection signals from the Q-DCO output is also added as a reference.



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	100 kHz	-80.83dBc/Hz			
2	N	1	1.00 MHz	-114.21dBc/Hz			
3	N	2	100 kHz	-74.46dBc/Hz			
4	N	2	1.00 MHz	-107.78dBc/Hz			
5	N	3	100 kHz	-68.49dBc/Hz			
6	N	3	1.00 MHz	-103.44dBc/Hz			

Fig. 7.11 Measured close loop phase noise at 6GHz, 12 GHz and 24 GHz outputs



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	1.00 MHz	-99.83dBc/Hz			
2	N	2	1.00 MHz	-94.07dBc/Hz			
3	N	3	1.00 MHz	-87.88dBc/Hz			
4	N	1	10.0 MHz	-119.85dBc/Hz			
5	N	2	10.0 MHz	-113.90dBc/Hz			
6	N	3	10.0 MHz	-104.73dBc/Hz			

Fig. 7.12 Measured close loop phase noise at 11.625 GHz, 23.25 GHz and 46.5 GHz outputs

7.4.5 Spur

Fig. 7.13 shows the measured reference spur at 6GHz output, where the reference spur is smaller than -50 dB.

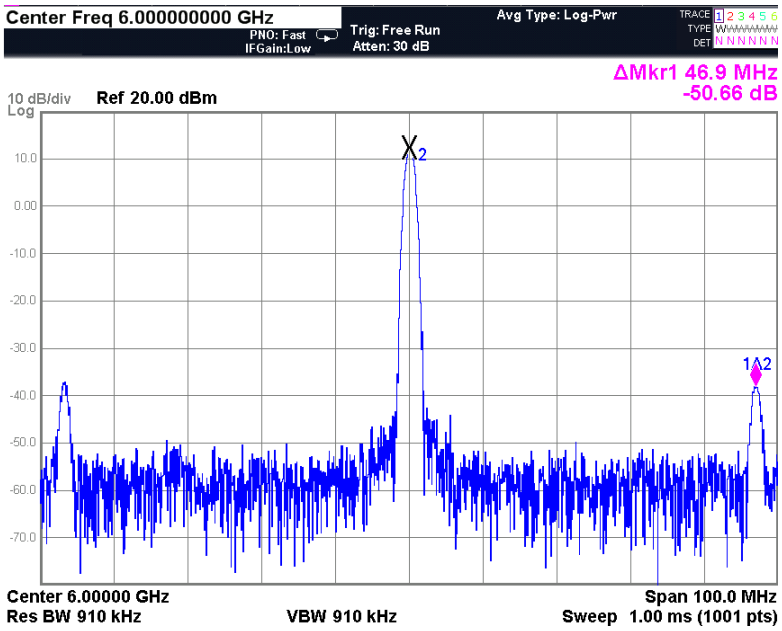


Fig. 7.13 Measured reference spur at 6 GHz output

7.4.6 IQ Mismatch

Fig. 7.14 shows the measured spectrum at the single sideband mixer (SSBM) output for 6 GHz LO signal. The sideband rejection is about 35 dB which corresponding to an IQ phase mismatch of 2^{o}.

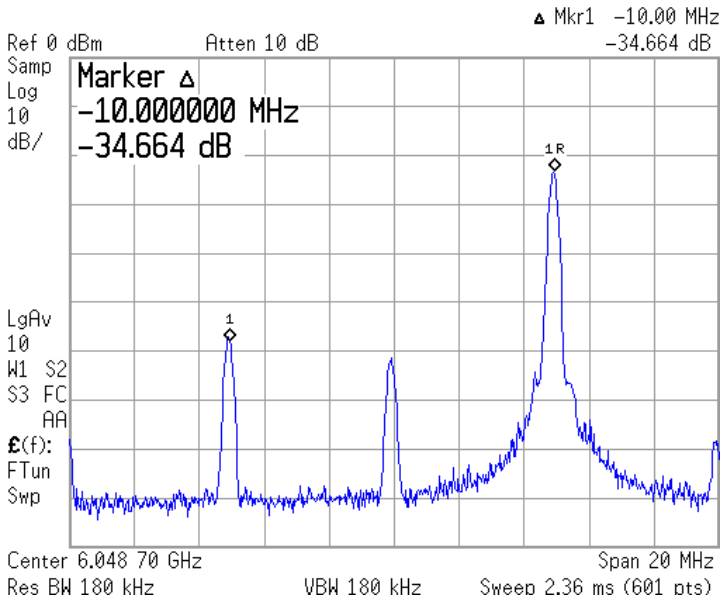


Fig. 7.14 Measured spectrum at the SSBM output for 6 GHz LO signal

Table 7.1 summarizes the measured performance of the proposed SDR all-digital frequency synthesizer, and compares it with the recently published state-of art wide-band frequency synthesizer.

7.4.7 Settling Time

Fig. 7.15 shows the measured settling time for WLAN (802.11a) standard. When jumped from 5380 MHz to 5420 MHz, the settling time is around 40 μs.

Fig. 7.16 shows the measured settling time for Bluetooth standard. When jumped from 2420 MHz to 2440 MHz, the settling time is around 60 μs.

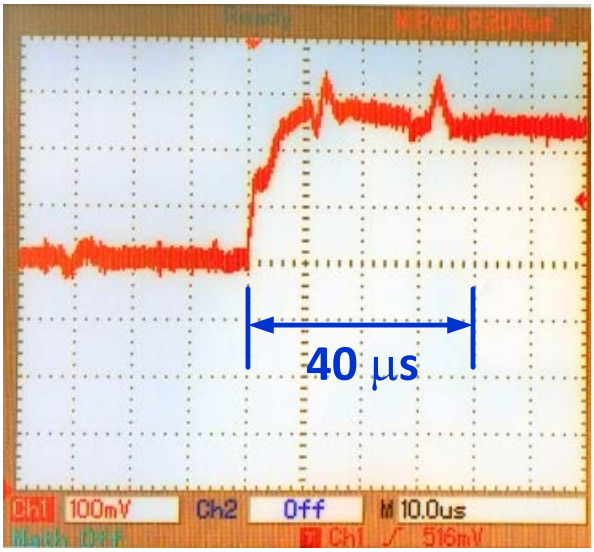


Fig. 7.15 Measured settling time for WLAN (802.11a) standard

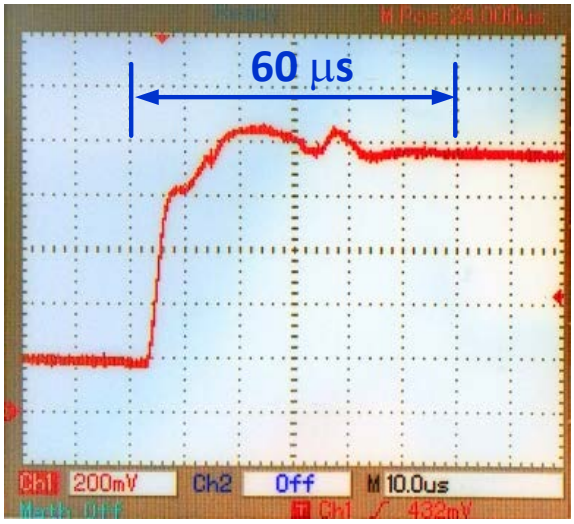


Fig. 7.16 Measured settling time for Bluetooth standard

Table 7.1 Performance summary and comparison of the SDR frequency synthesizer

	Tech.	Freq. Range (GHz)	Power (mW)	Phase Noise (In-band) (dBc/Hz)	Phase Noise@1MHz (dBc/Hz)	Active Area (mm^2)
This Work	**65nm CMOS**	**0.306 – 23.25 (IQ) 23.25 – 46.5 (Diff.)**	**30(1) ~ 80(2)**	**-100 (1.8GHz) -78 (40GHz)**	**-126 (1.8GHz) -95.4 (40GHz)**	**2.2**
ISSCC 2011 [4]	0.13µm CMOS	0.047 – 10 (IQ) 19 – 22 (IQ) 38 – 44 (IQ)	33 ~ 83	-98 (1.8GHz) -70 (40GHz)	-130.1 (1.8GHz) -92 (40GHz)	3
JSSC 2010 [5]	40nm CMOS	5.5 – 6 (IQ) 6 – 12 (Diff.)	30	-90 (1.8GHz)	-129 (1.8GHz)	0.5
JSSC 2011 [6]	90nm CMOS	5 – 10 (IQ) 10 – 32 (Single)	104 ~ 126	-	-131 (1.8GHz)(3)	1.67

(1) RF frequency output, (2) mm-Wave frequency output, (3) using external PLL to generate the injection signal.

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Chapter 8

Conclusion and Future Research

8.1 Thesis Summary

In this dissertation, circuit techniques and system architectures are investigated to realize a wideband LO SDR frequency synthesizer for software-defined radios.

For the innovated circuit techniques, chapter 3 proposed a wide-band VCO based on the switched-transformer technique. By using the common mode switches, the frequency tuning range of the conventional dual-band VCO is increased. What' more important is the new mode created by the common mode switches is located between the low band and high band of the conventional dual-band VCO, which makes the entire frequency tuning range to be continuous. The experimental results show that the triple-mode VCO achieves a frequency tuning range from 4.5 to 13.4 GHz, which is enough to cover the 6 to 12 GHz frequency band required by the proposed SDR frequency synthesizer architecture. The measured phase noise performance at 7.3 GHz carrier can satisfy all the requirements from the specifications derived in Chapter 2. The triple-mode VCO using the switched-transformer technique is the heart of the proposed SDR frequency synthesizer architecture. Based on this switch-transformer technique, the wide-band DCO is proposed in Chapter 4 by adding the capability of fine digital frequency tuning to make it suitable for the ADPLL loop. Furthermore, the wide-band DCO is further expanded to a Q-DCO by coupling the two DCOs together to generate the IQ signals that required by the ILFM in the mm-Wave frequency synthesis part.

In Chapter 5, a switched-triple-shielded transformer is proposed to effectively change the magnetic coupling coefficient in a transformer-based dual-band VCO to increase the frequency tuning range. Based on the proposed switched-triple-shielded transformer, a magnetically-tuned multi-mode mm-Wave VCO with ultra-wide frequency tuning range is successfully demonstrated in 65 nm CMOS process. Drawing 7 mA to 9 mA at 1.2 V supply, the presented multi-mode VCO achieves a continuous ultra-wide frequency tuning range of 44.2% from 57.5 to 90.1 GHz while still occupying small chip area with a single multiple-port transformer. The measured phase noise across the entire frequency range is between -104.6 to -112.2 dBc/Hz @10 MHz frequency offset, corresponding to FOM_T between -184.2 and -192.2 dBc/Hz. The switched-triple-shielded transformer is the key technique in the mm-Wave frequency synthesis part. Later, the ×4 ILFM proposed in Chapter 7 will use it to achieve wide frequency tuning range from 24 to 48 GHz.

In Chapter 6, a SFT transformer-based ILFD with enhanced frequency locking range is successfully demonstrated. By creating a frequency-dependent phase shift for the total current injected into the transformer tank, the SFT technique helps relax both the phase and gain conditions, thus increase the locking range of the ILFD. Implemented in 65nm CMOS, the presented frequency divider occupies a core area of 0.22×0.11 mm^2. When consuming 1.9 mW from 0.8 V supply, it achieves an input locking range of 29% from 53.7 to 72.0 GHz at 0 dBm input power and a corresponding FOM of 9.53, which to the best of our knowledge, is the highest reported to date among all the published CMOS frequency divider at 60 GHz. In the mm-Wave frequency synthesis part, two SFT ILFDs are employed to cover the input frequency range from 33

to 34 GHz and 32 to 50 GHz, respectively, which can generate IQ LOs by dividing down the ILFM outputs.

Enabled by the proposed circuit techniques, the SDR frequency synthesizer system is implemented and demonstrated. In Chapter 4, the 1.5 to 12 GHz ADPLL is proposed by using a hybrid PTDC to achieve low phase noise and spur performance. The proposed PTDC achieves an improved linearity and reduced area and power consumption by narrowing the input range with the help of the 8-phase inputs generated by the frequency division from the DCO operating at much higher frequency.

Finally, in Chapter 7, the whole picture of the proposed SDR all-digital frequency synthesizer is illustrated and discussed. Fabricated in the 1P9M 65-nm CMOS technology, it can generate IQ LOs from 305 MHz to 23.25 GHz and differential LOs from 23.25 to 46.5 GHz with required phase noise performance specified by all the wireless standards. The output frequency can be further divided down to generate IQ LOs below 305 MHz easily by using the dynamic divider if required.

8.2 Future Research

The main focus and contributions of this work are the generation of LO frequency from DC to the mm-Wave frequency continuously. Nevertheless, there are still many topics that are interesting and worth exploring to expand the SDR frequency synthesizer system.

One issue that can be explored is how to support the standards such as the multi-band OFDM UWB standard located at frequency band from 3.1 to 10.6 GHz, which requires a very fast channel hopping time less than 9.47 ns. Such a fast channel hopping time can only be achieved by using single-sideband mixing method in an open loop

manner. Since the proposed SDR frequency synthesizer already provides the IQ frequency from DC to 24 GHz, investigation can be conducted to find a optimized way to utilized the existing IQ frequency to synthesize the LOs for the UWB standard, which requires in low power consumption and small chip area.

Another interesting aspect is to further expand the SDR frequency synthesizer to even higher frequency. In this work, the LO generation is only up to 48 GHz. One way to expand the LO frequency to higher frequency is to cascade more frequency multipliers after it. However, the frequency alignment at that high frequency will be a severe problem and needs to be carefully addressed.

The performance requirements for different wireless standards are quite different, for some low end standards such as Zigbee and Bluetooth, it requires low power consumption with a rather relaxed phase noise performance. This can be achieved by decrease the current consumption of the DCO and reconfigure the loop bandwidth. In this work, all these adjustment is performed manually. It will be an interesting topic if we can automatically detect the performance parameter of frequency synthesizer like the phase noise and spur level. And then we only needs to set the requirements on these parameters and the frequency synthesizer will automatically change the bias condition and loop parameters to satisfy the performance.

Appendix-I

Equations for the Multi-Coil Transformer

For the n-coil transformer with magnetic coupling coefficient k_{ij} between either two coils L_i and L_j as shown in Fig. I-1, from the law of electromagnetic induction, the induced voltage in the ith coil can be expressed as below:

$$\varepsilon_i = -N\frac{\mathrm{d}\sum_{j=1}^{n}\Phi_{ij}}{\mathrm{d}t} = \sum_{j=1}^{n}\left(-N\frac{\mathrm{d}\Phi_{ij}}{\mathrm{d}i_j}\frac{\mathrm{d}i_j}{\mathrm{d}t}\right) \tag{A1}$$

$$-N\frac{\mathrm{d}\Phi_{ij}}{\mathrm{d}i_j} = L_i(i=j) \text{ or } M_{ij}\ (i\neq j) \tag{A2}$$

where L_i is the self-inductance of the ith coil, Φ_{ij} is the magnetic flux through the coil L_i induced by the coil L_j, and $M_{ij} = M_{ji} = k_{ij}\sqrt{L_i L_j}$ is the mutual-inductance between the ith and jth coils. By putting (A2) into (A1) and applying the Laplace transformation, the V-I equation for the ith coil can be expressed as:

$$V_i = sL_iI_i + \sum_{j=1, j\neq i}^{n}\left(M_{ij}I_j\right) \tag{A3}$$

Extending the results in Eq. (A3) to the switched-tripled-shielded transformer as shown in Fig. 5.5 to get:

$$V_1 = \left(sL_1 + R_{L1}\right)I_1 + sM_{12}I_2 + sM_{1A}I_A + sM_{1B}I_B \tag{A4}$$

$$V_2 = \left(sL_2 + R_{L2}\right)I_2 + sM_{12}I_1 + sM_{2A}I_A + sM_{2C}I_C \tag{A5}$$

$$V_A = \left(sL_A + R_{LA}\right)I_A + sM_{1A}I_1 + sM_{2A}I_2 = -I_A Z_A \tag{A6}$$

$$V_{\mathrm{B}} = \left(sL_{\mathrm{B}} + R_{\mathrm{LB}}\right) I_{\mathrm{B}} + sM_{1\mathrm{B}} I_1 = -I_{\mathrm{B}} Z_{\mathrm{B}} \tag{A7}$$

$$V_{\mathrm{C}} = \left(sL_{\mathrm{C}} + \mathrm{R}_{\mathrm{LC}}\right) I_{\mathrm{C}} + sM_{2\mathrm{C}} I_2 = -I_{\mathrm{C}} Z_{\mathrm{C}} \tag{A8}$$

Here, the coupling between L_A and L_B, L_A and L_C are ignored because they do not affect L_1 and L_2 directly. By putting Eqs. (A6)-(A8) into Eqs. (A4)-(A5), the voltages V_1 and V_2 as functions of I_1 and I_2 can be expressed as:

$$V_1 = \left(sL_1 + R_{\mathrm{L1}} - \frac{s^2 M_{1\mathrm{A}}^2}{sL_{\mathrm{A}} + R_{\mathrm{LA}} + Z_{\mathrm{A}}} - \frac{s^2 M_{1\mathrm{B}}^2}{sL_{\mathrm{B}} + R_{\mathrm{LB}} + Z_{\mathrm{B}}} \right) I_1 + \left(sM_{12} - \frac{s^2 M_{1\mathrm{A}} M_{2\mathrm{A}}}{sL_{\mathrm{A}} + R_{\mathrm{LA}} + Z_{\mathrm{A}}} \right) I_2 \tag{A9}$$

$$V_2 = \left(sL_2 + R_{\mathrm{L2}} - \frac{s^2 M_{2\mathrm{A}}^2}{sL_{\mathrm{A}} + R_{\mathrm{LA}} + Z_{\mathrm{A}}} - \frac{s^2 M_{2C}^2}{sL_{\mathrm{C}} + R_{\mathrm{LC}} + Z_C} \right) I_2 + \left(sM_{12} - \frac{s^2 M_{1\mathrm{A}} M_{2\mathrm{A}}}{sL_{\mathrm{A}} + R_{\mathrm{LA}} + Z_{\mathrm{A}}} \right) I_1 \tag{A10}$$

By replacing s with jω and Z_A, Z_B, Z_C with $R_{on,A}$, $R_{on,A}$, $R_{on,A}$ or $1/\omega C_{off,A}$, $1/\omega C_{off,B}$, $1/\omega C_{off,C}$ in the three different states properly, Eqs. (A9) and (A10) can be simplified as:

$$V_1 = \left(L_1' + R_{\mathrm{L1}}'\right) I_1 + sM_{12}' I_2 + R_{\mathrm{M}}' I_2 \tag{A11}$$

$$V_2 = \left(L_2' + R_{\mathrm{L2}}'\right) I_2 + sM_{12}' I_1 + R_{\mathrm{M}}' I_1 \tag{A12}$$

In (A11), the effect of Z_A on the effective series resistance of L'_1 through the coupling from L_A to L_1 has already been absorbed into the term R'_{L1}. The term $R'_M I_2$ represents the effect of Z_A on the equivalent series resistance of L'_1 through coupling from L_A to L_2 to L_1 because this term becomes zero if the secondary coil is open. As a result, the term $R'_M I_2$ can be ignored when k_{1A}, k_{2A} and k_{12} are small. Because of the symmetric property for V_2 and V_1, the term $R'_M I_1$ in (A12) can also be neglected for the same reason. Consequently, the simplified model for the switched-triple-shielded transformer shown in Fig. 5.4 can be obtained, and the effective parameters L_1', L_2', R_1', R_2', and k_{12}' for the three states can be derived as expressed in Eqs. (4a)-(5e) and (8a)-

(8e). Furthermore, by making $k_{1B} = k_{2C} = 0$, the parameters L_1', L_2', and k_{12}' of the switched-single-shielded transformer can be derived as expressed in Eqs. (2a)-(3c).

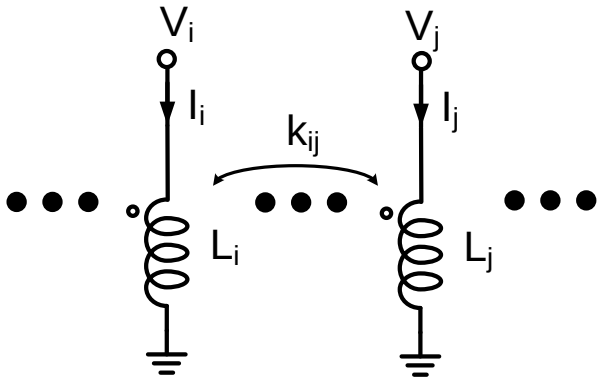

Fig. I-1 Schematic of the multi-coil transformer

Appendix-II

Passive Device Simulation and Characterization

Fig. II-1 shows the typical flow for the design of inductors and inductors.

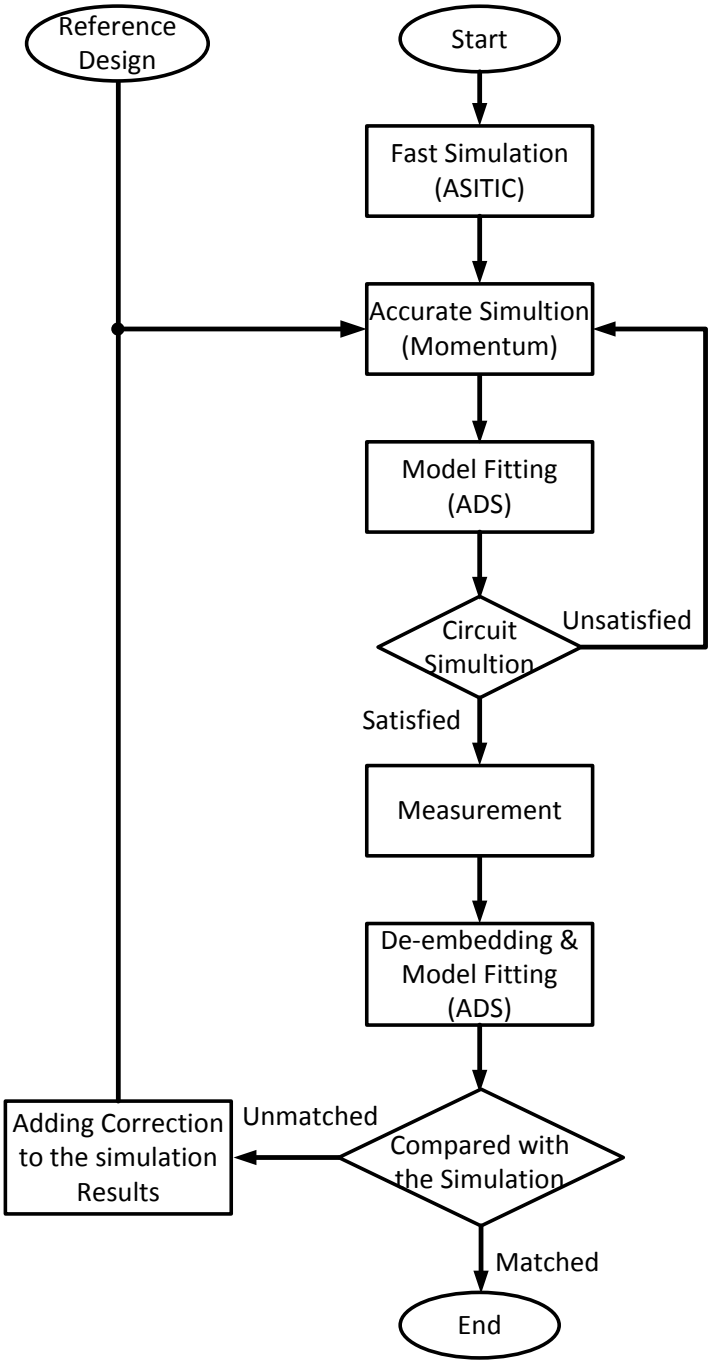

Fig. II-1 Design flow of inductors or transformers

At the beginning, the key parameters of inductors or transformers can be quickly estimated and optimized by using the fast simulator such as ASITIC [1]. In the optimization, different layout configurations can be tried and the physical parameters such as the turn number, the diameter, metal width, the line spacing and the space between the primary and secondary coils of the transformer can be adjusted. However, the estimated Q from ASITIC is usually much higher than the actual Q. So in this stage, we just focus on the relatively Q for different parameter combinations.

After obtain the basic physical parameters from ASITIC, the inductors or the transformers are then simulated by using the 2.5D EM simulator Momentum in the ADS. In this stage, the physical parameters can be finely tuned to obtain the most optimized design that can satisfy the requirements. The simulated S parameters will be converted into the Y and Z parameters first. Then to obtain the inductance L and the quality factor Q of the inductor, the following equations can be employed:

$$L=\frac{\mathrm{Im}\,(Z_1)}{\omega} \tag{B1}$$

$$Q=\frac{\mathrm{Im}\,(Z_1)}{\mathrm{Re}\,(Z_1)} \tag{B2}$$

where $\omega=2\pi f$. And to obtain the inductance L_1 and L_2 and the quality factor Q_1 and Q_2 of the primary and secondary coils, respectively and the coupling coefficient k between the primary and secondary coils for the transformer, the following equations can be employed:

$$L_1=\frac{\mathrm{Im}\,(Z_{11})}{\omega} \tag{B3}$$

$$L_2=\frac{\mathrm{Im}\,(Z_{22})}{\omega} \tag{B4}$$

$$Q_1 = \frac{\mathrm{Im}\,(Z_{11})}{\mathrm{Re}\,(Z_{11})} \tag{B5}$$

$$Q_2 = \frac{\mathrm{Im}\,(Z_{22})}{\mathrm{Re}\,(Z_{22})} \tag{B6}$$

$$k = \sqrt{\frac{\left(Y_{11}^{-1} - Z_{11}\right) Z_{22}}{\mathrm{Im}(Z_{11})\mathrm{Im}(Z_{22})}} \tag{B7}$$

After the design is fixed, the simulated S-parameter data from Momentum will be fitted by using the circuit models for inductors or transformers as shown in Fig. II-2 and Fig. II-3. After the circuit model is obtained, it can be used for transistor level simulation in the spectreRF. If the circuit simulation results are what we expected, we can use this inductor or transformer in the circuits and also build the testing structures for it as well. If the circuit simulation results are not satisfied, then we may need to go back to momentum for some design iterations.

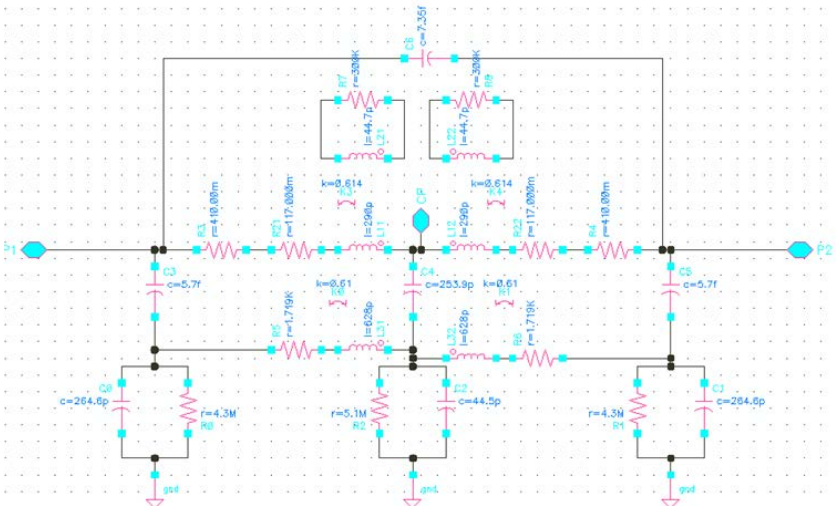

Fig. II-2 Wide-band inductor model for circuit simulation

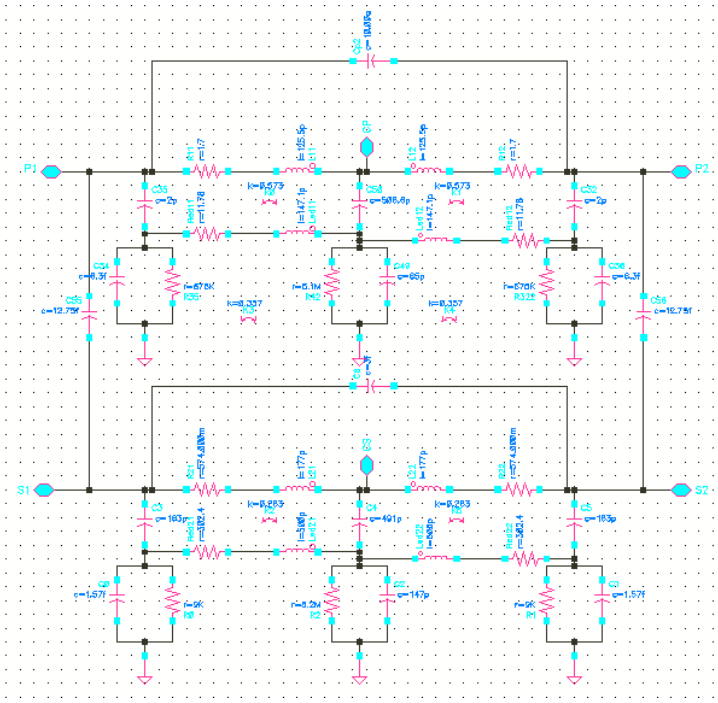

Fig. II-3 Wide-band transformer model for circuit simulation

After the tape-out, the testing structures of the inductor or transformer are measured based on the on-wafer probing.

1) Inductor Measurement: Fig. II-4 shows the layout of the inductor testing structure and the open-short structures for de-embedding purpose. Here, since our network analyzer can only do the single-ended measurement, one terminal of the inductor is connected to the ground plane to configure the inductor for single-ended measurement.

   After the measured S parameter of the inductor DUT, open and short structures has been obtained, the following de-embedding procedures can be applied to get the inductance and Q value of the desired inductor [2]:

   Open correction of short:

   $Y_{short\_cor} = Y_{short} - Y_{open}$

Open correct of the inductor DUT:

$$Y_{IND\_cor} = Y_{IND} - Y_{open}$$

Short correction of the inductor DUT:

$$Z_{IND\_cor} = ytoz(Y_{IND\_cor})$$

$$Z_{short\_cor} = ytoz(Y_{short\_cor})$$

$$Z_{IND\_Deemb} = Z_{IND\_cor} - Z_{short\_cor}$$

Once the Z_{IND_Deemb} is obtained, the measured inductance L_{mea} and quality factor Q_{mea} can be obtained by replace the Z_1 with Z_{IND_Deemb} in Eqns. (B1) and (B2).

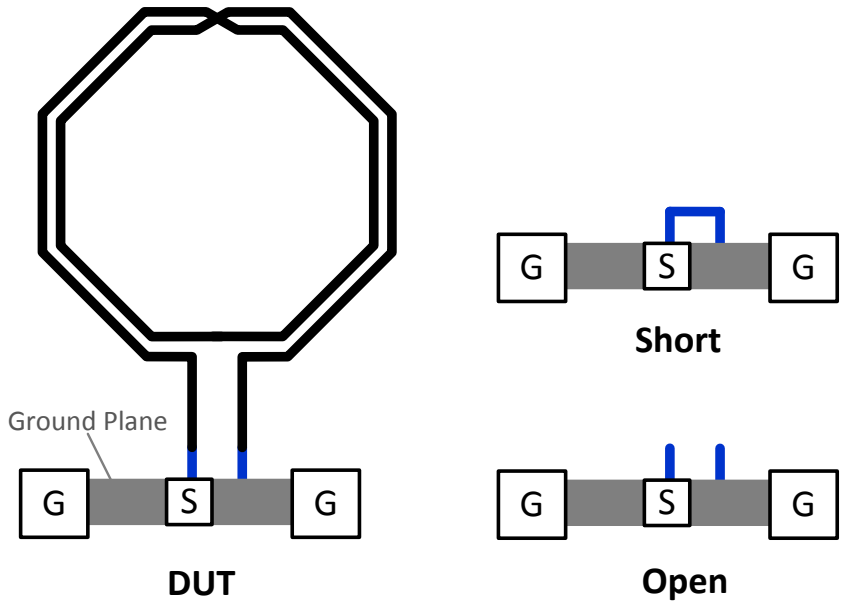

Fig. II-4 Layout of the inductor testing structure and open-short calibration structures for de-embedding.

2) Transformer Measurement: Fig. II-5 shows the layout of the transformer testing structure and the open-short structures for de-embedding purpose. For the

transformer, two open and short de-embedding structures are needed for both primary and secondary coils

After the measured S parameter of the transformer DUT, open and short structures has been obtained, the following de-embedding procedures can be applied to get the inductance, Q value and coupling coefficient k of the desired transformer:

Open correction of shorts:

$$Y_{short\_cor,11} = Y_{short,11} - Y_{open,11}$$

$$Y_{short\_cor,22} = Y_{short,22} - Y_{open,22}$$

Open correct of the transformer DUT:

$$Y_{TF\_cor,11} = Y_{TF,11} - Y_{open,11}$$

$$Y_{TF\_cor,22} = Y_{TF,22} - Y_{open,22}$$

Short correction of the transformer DUT:

$$Z_{TF\_cor} = ytoz(Y_{TF\_cor})$$

$$Z_{short\_cor} = ytoz(Y_{short\_cor})$$

$$Z_{TF\_Deemb,11} = Z_{TF\_cor,11} - Z_{short\_cor,11}$$

$$Z_{TF\_Deemb,22} = Z_{TF\_cor,22} - Z_{short\_cor,22}$$

$$Y_{TF\_Deemb} = ztoy(Z_{TF\_Deemb})$$

Once the Z_{TF_Deemb} and Y_{TF_Deemb} are obtained, the measured inductance $L_{1,mea}$, $L_{2,mea}$, quality factor $Q_{1,mea}$ $Q_{2,mea}$ and coupling coefficient k_{mea} can be obtained by replacing the Z_{11}, Z_{22} and Y_{11} with $Z_{TF\_Deemb,11}$ and $Z_{TF\_Deemb,22}$ and $Y_{TF\_Deemb,11}$ in Eqns. (B3)-(B7).

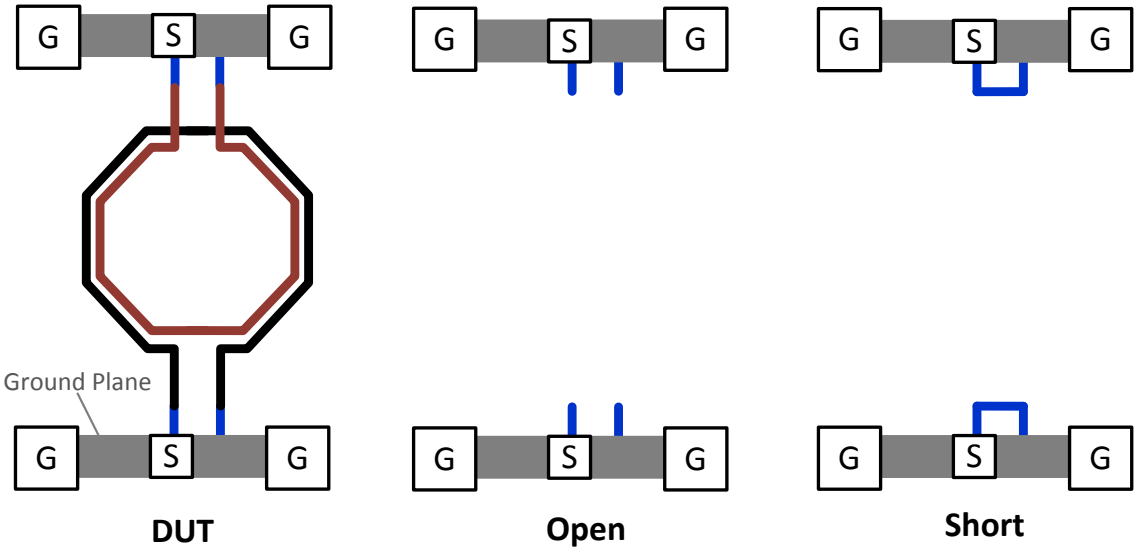

Fig. II-5 Layout of the transformer testing structure and open-short calibration structures for de-embedding.

Finally, the measured results of the inductor or the transformer are compared with the simulation results. The difference can be used to correct the simulation results for later tape-out.

Bibliography

[1] http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

[2] F. Gianesello, Y. Morandini, S. Boret, D. Gloria, "Characterization and Model Parameter Extraction of Symmetrical Centre Tapped Inductor using Build in Mixed Mode and Pure Differential S-Parameters," *IEEE Microelectronic Test Structures International Conf.*, pp. 181-183, 2009.

Appendix-III

List of Publications

Conference papers:

1. **Jun Yin**, H. C. Luong, "A 57.5-to-90.1GHz Magnetically-Tuned Multi-Mode CMOS VCO," *IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, Sept 2012.
2. **Jun Yin** and H. C. Luong, "A 0.8V 1.9mW 53.7-to-72.0GHz Self-Frequency-Tracking Injection-Locked Frequency Divider," *IEEE Radio-Frequency Integrated Circuits Symposium (RFIC)*, Montreal, pp. 305-308, Jun. 2012.
3. **Jun Yin**, J. Yi, M. Law, M. Ling, P. Lee, B. Ng, B. Gao, H. C. Luong, A. Bermak, M. Chan, W. H. Ki, C. Y. Tsui, M. Yuen, "A System-on-Chip EPC Gen-2 Passive UHF RFID Tag with Embedded Temperature Sensor," *IEEE International Solid-State Circuit Conference 2010 (ISSCC)*, San Francisco, Feb. 2010.

Journal papers:

1. **Jun Yin,** J. Yi, M. Law, M. Ling, P. Lee, B. Ng, B. Gao, H. C. Luong, A. Bermak, M. Chan, W. H. Ki, C. Y. Tsui, M. Yuen, "A System-on-Chip EPC Gen-2 Passive UHF RFID Tag with Embedded Temperature Sensor," *IEEE Journal of Solid-State Circuits (JSSC)*, Nov. 2010.
2. **Jun Yin** and H. C. Luong, "A 57.5-to-90.1GHz Magnetically-Tuned Multi-Mode CMOS VCO," *IEEE Journal of Solid-State Circuits (JSSC)*, submitted in December 2012.

3. S. Rong**, J. Yin** and H. C. Luong, "A 0.05-to-10GHz 19-to-22GHz and 38-to-44GHz SDR Frequency Synthesizer in 0.13μm CMOS," *IEEE Journal of Solid-State Circuits (JSSC)*, to be submitted in Feb 2013.
4. **Jun Yin** and H. C. Luong, "A DC to 48GHz All-Digital Frequency Synthesizer for Software-Defined Radios," *IEEE Journal of Solid-State Circuits (JSSC)*, to be submitted in March 2013.

Patents:

1. **Jun Yin** and H. C. Luong, "Magnetically Frequency Tuning Technique for Millimeter Wave VCO," *US patent*, to be filed.